

FEATURES

- Fast Response Time 180ns Max
- High Input Slew Rate 92V/ μ s
- Low Offset Voltage 0.3mV Typical, 0.8mV Max
- Low Offset Current 4nA Typical, 25nA Max
- Low Offset Drift 1 μ V/ $^{\circ}$ C, 30pA/ $^{\circ}$ C
- Standard Power Supplies +5V or $\pm$ 5V to $\pm$ 18V
- Guaranteed Operation from Single +5V Supply
- No Pull-Up Resistor Required for TTL Drive
- Wired OR Capability
- Fits 111, 106, 710 Sockets
- Easy Offset Nulling Single 2k Ω Potentiometer
- Easy to Use Free from Oscillations
- Available in Die Form

ORDERING INFORMATION [†]

T _A = +25 $^{\circ}$ C V _{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	
0.8	CMP01J*	CMP01Z/883	—	MIL
0.8	CMP01EJ	CMP01EZ	CMP01EP	COM
2.8	CMP01CJ	CMP01CZ	CMP01CP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

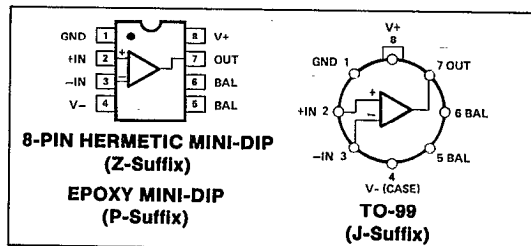
[†] Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

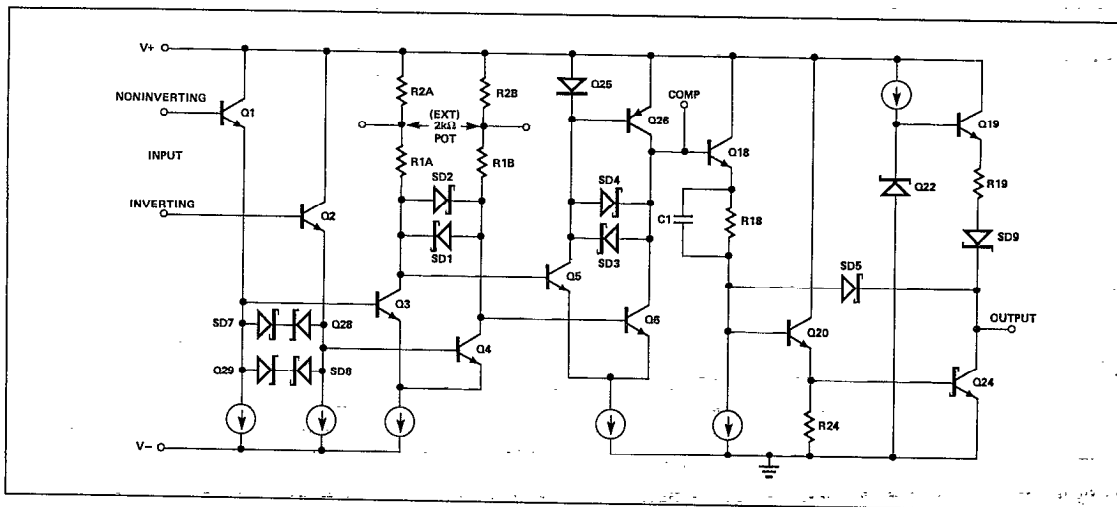
The CMP-01 is a monolithic fast precision voltage comparator using an advanced NPN-Schottky Barrier Diode process. It features fast response time to both large and small input signals, while maintaining excellent input characteristics. The CMP-01 is capable of operating over a wide range of supply voltages including single ended 5 volt supply. The large output current sinking and high output voltage capability assure good application flexibility, while the combination of fast response, high accuracy, and freedom from oscillation assure performance in precision level detectors and 12 and 13-bit A/D converters. The CMP-01 is pin-compatible to earlier 111, 106, and 710 types. For applications requiring lower input offset and bias currents, refer to the CMP-02 data sheet.

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PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



CMP-01

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage, V_+ to V_-	36V
Output to Ground	-5V to +32V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Positive Supply Voltage to Ground	+30V
Positive Supply Voltage to Offset Null	0 to 2V
Differential Input Voltage	$\pm 11V$
Input Voltage ($V_S = \pm 15V$)	$\pm 15V$
Output Sink Current (Continuous Operation)	75mA
Operating Temperature Range	
CMP-01	-55°C to +125°C
CMP-01E, CMP-01C	0°C to +70°C
Junction Temperature (T_J)	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
P-Suffix	-65°C to +125°C

Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration	
To Ground	Indefinite
To V_+	1 Minute

PACKAGE TYPE	θ_{JA} (Note 2)	θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Plastic DIP (P)	148	16	°C/W
8-Pin SO (S)	103	43	°C/W

NOTES:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO and P-DIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01 CMP-01E			CMP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.3	0.8	—	0.4	2.8	mV
Input Offset Current	I_{OS}	(Note 1)	—	4	25	—	5	80	nA
Input Bias Current	I_B		—	350	600	—	400	900	nA
Differential Input Resistance	R_{IN}	(Note 2)	150	300	—	100	200	—	k Ω
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	200	500	—	100	500	—	V/mV
Response Time (Note 3)	t_r	100mV step, 5mV Overdrive	—	—	—	—	—	—	ns
		No Load (No Pull-Up)	—	110	180	—	110	180	
		5k Ω to 5V (Pull-Up)	—	110	—	—	110	—	
		TTL Fan-Out = 4, No Pull-Up	—	110	—	—	110	—	
		5V Step 5mV Overdrive	—	160	—	—	160	—	
		No Load (No Pull-Up)	—	160	—	—	160	—	
		5k Ω to 5V (Pull-Up)	—	160	—	—	160	—	
		TTL Fan-Out = 4, No Pull-Up	—	160	—	—	160	—	
Input Slew Rate			—	92	—	—	92	—	V/ μs
Input Voltage Range	CMVR		± 12.5	± 13	—	± 12.5	± 13	—	V
Common-Mode Rejection Ratio	CMRR		94	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	—	74	98	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$	2.4	3.2	—	—	—	—	V
		$V_{IN} \geq 3mV$, $I_O = 240\mu A$	—	—	—	2.4	3.4	—	
		$V_{IN} \geq 3mV$, $I_O = 0mA$	2.4	4.8	—	2.4	4.8	—	
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0mA$	—	0.16	0.4	—	0.16	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.31	0.45	
		$V_{IN} \leq -10mV$, $I_{sink} \leq 12mA$ (CMP-01 only)	—	0.36	0.5	—	—	—	
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = +30V$	—	0.03	2	—	0.05	8	μA
Positive Supply Current	I_+	$V_{IN} \leq -10mV$	—	5.6	8	—	5.6	8.5	mA
Negative Supply Current	I_-	$V_{IN} \leq -10mV$	—	1.3	2.2	—	1.3	2.2	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	103	153	—	103	161	mW
Offset Voltage Adjustment Range		Nulling Pot $\geq 2k\Omega$	—	± 5	—	—	± 5	—	mV

NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_{S+} = 5V$, $V_{S-} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01 CMP-01E			CMP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	3	21	—	4	65	nA
Input Bias Current	I_B		—	250	500	—	300	720	nA
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	—	50	—	—	50	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive	—	150	—	—	150	—	ns
		5k Ω to 5V (Pull-Up) TTL Fan-Out = 4, 5k Ω to 5V (Pull-Up)	—	150	—	—	150	—	
Input Voltage Range	CMVR		1.8	1.7-3.8	3.5	1.8	1.7-3.8	3.5	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I_+	$V_{IN} \leq -10mV$	—	2.3	3.2	—	2.4	3.8	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	11.5	16	—	12	19	mW

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ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1) $V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.5	1.6	mV
Average Input Offset Voltage Drift			—	0.6	2.8	
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	$\mu V/^\circ C$
With External Trim	TCV_{OSn}		—	1	—	
Input Offset Current	I_{OS}	$T_A = +125^\circ C$, (Note 1) $T_A = -55^\circ C$, (Note 1)	—	4	25	nA
Average Input Offset Current Drift	TCI_{OS}	$+25^\circ C \leq T_A \leq +125^\circ C$ $-55^\circ C \leq T_A \leq +25^\circ C$	—	5	45	
Input Bias Current	I_B	$T_A = +125^\circ C$	—	12	—	$pA/^\circ C$
		$T_A = -55^\circ C$	—	35	—	
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	—	330	600	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive, (Note 2) $T_A = +125^\circ C$, No Load $T_A = -55^\circ C$, No Load	—	550	1400	
Input Voltage Range	CMVR		—	100	—	ns
Common-Mode Rejection Ratio	CMRR		—	220	—	
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	—	100	—	V
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	—	88	106	
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0mA$ $V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	75	96	dB
			—	2.4	3	
			—	0.20	0.4	V
			—	0.32	0.5	

NOTES:

- These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
- Guaranteed by design.

CMP-01

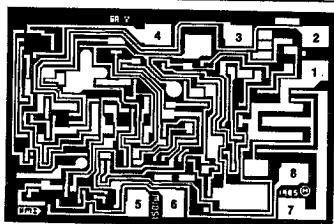
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01E			CMP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1) $V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.4 0.5	1.4 2.4	—	0.5 0.6	3.5 4.3	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	$\mu V/^\circ C$
With External Trim	TCV_{OSn}		—	1.0	—	—	1.2	—	
Input Offset Current	I_{OS}	$T_A = +70^\circ C$, (Note 1) $T_A = 0^\circ C$, (Note 1)	—	4 5	25 45	—	5 6	80 120	nA
Average Input Offset Current Drift	TCI_{OS}	$+25^\circ C \leq T_A \leq +70^\circ C$ $0^\circ C \leq T_A \leq +25^\circ C$	—	12 35	—	—	12 40	—	$pA/^\circ C$
Input Bias Current	I_B	$T_A = +70^\circ C$ $T_A = 0^\circ C$	—	330 400	600 950	—	340 450	900 1200	nA
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive $T_A = +70^\circ C$, No Load $T_A = 0^\circ C$, No Load	—	150 100	—	—	150 100	—	ns
Input Voltage Range	CMVR		± 12.0	± 13.3	—	± 12.0	± 13.3	—	V
Common-Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0$ $V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.17 0.3	0.4 0.5	—	0.17 0.31	0.4 0.5	V

NOTES:

- These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
- Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.065×0.043 inch, 2730 sq. mils
(1.651×1.092 mm, 1.803 sq. mm)

1. GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$.

3

PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	0.8	2.8	mV MAX
Input Offset Current	I_{OS}	(Note 1)	25	80	nA MAX
Input Bias Current	I_B		600	900	nA MAX
Differential Input Resistance	R_{IN}	(Note 2)	150	100	k Ω MIN
Input Voltage Range	CMVR		± 12.5	± 12.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S \leq 18V$ $-18V \leq V_S \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4	—	V MIN
Saturation Voltage	V_{OL}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	2	8	μA MAX
Positive Supply Current	I_+	$V_{IN} \leq -10mV$	8.0	8.5	mA MAX
Negative Supply Current	I_-	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

WAFER TEST LIMITS at $V_{S+} = 5V$ and $V_{S-} = 0V$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		21	65	nA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

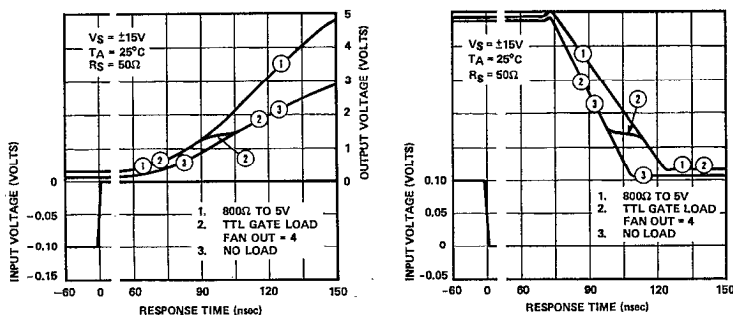
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N TYPICAL	CMP-01GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	1.5	1.8	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		35	40	pA/°C
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up), $T_A = 25^\circ C$	110	110	ns

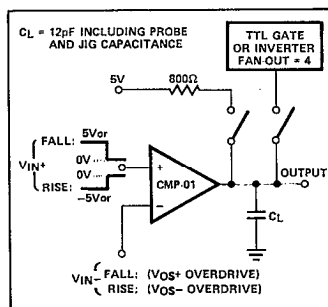
CMP-01

TYPICAL PERFORMANCE CHARACTERISTICS

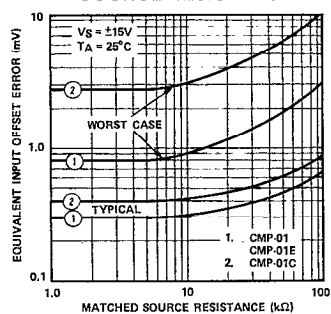
**RESPONSE TIME,
100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS**



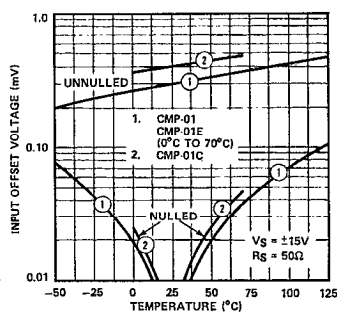
RESPONSE TIME TEST CIRCUIT



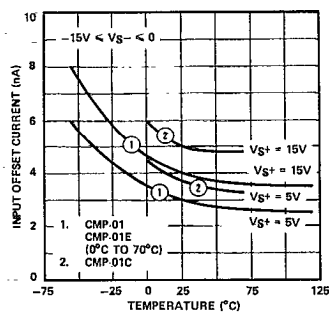
**INPUT OFFSET ERROR vs
SOURCE RESISTANCE**



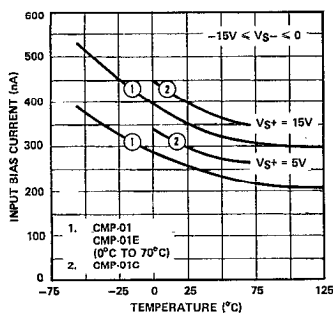
**OFFSET VOLTAGE vs
TEMPERATURE**



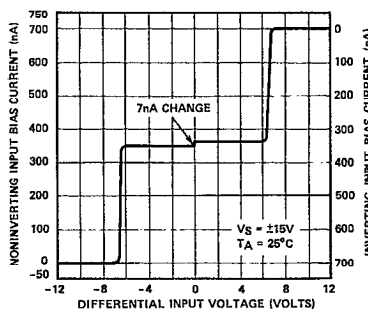
**INPUT OFFSET CURRENT
vs TEMPERATURE**



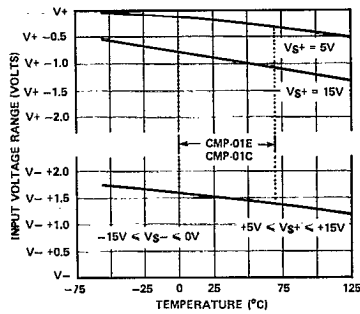
**INPUT BIAS CURRENT
vs TEMPERATURE**



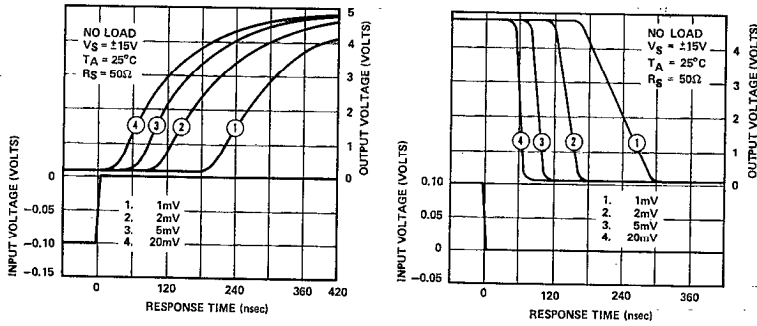
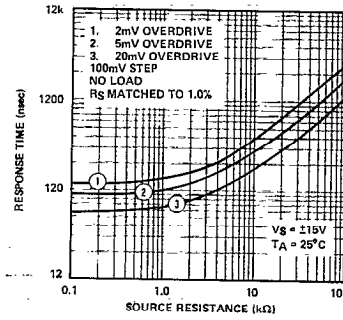
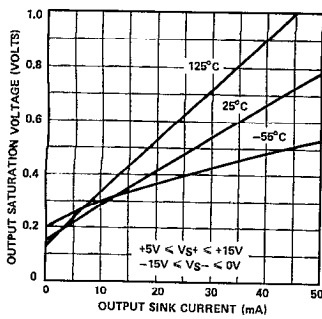
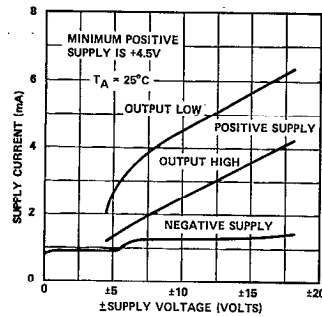
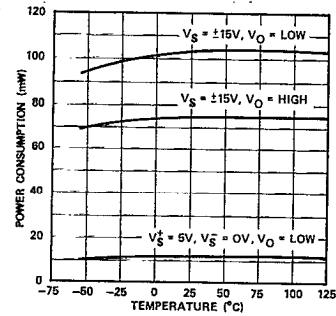
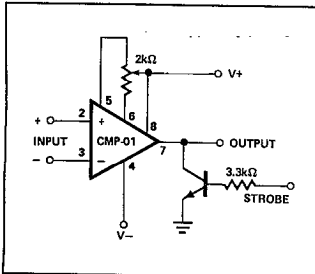
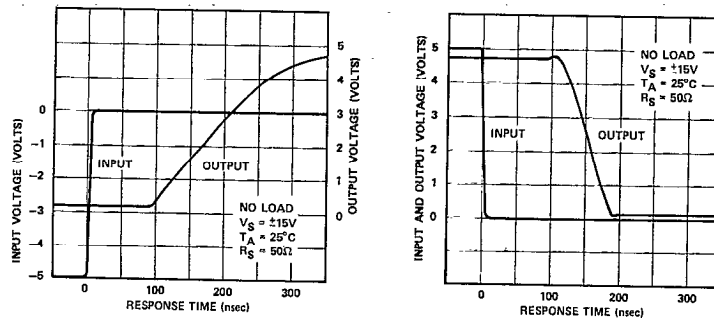
**INPUT BIAS CURRENT
vs DIFFERENTIAL
INPUT VOLTAGE**



**INPUT VOLTAGE RANGE
vs TEMPERATURE**



TYPICAL PERFORMANCE CHARACTERISTICS

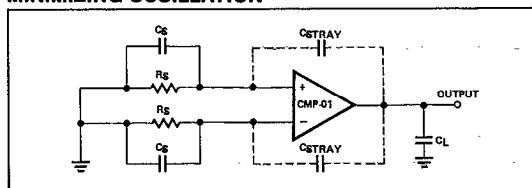
**RESPONSE TIME
FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES**

**RESPONSE TIME vs
SOURCE RESISTANCE**

**SATURATION VOLTAGE
vs SINK CURRENT**

**SUPPLY CURRENT vs
SUPPLY VOLTAGE**

**POWER CONSUMPTION
vs TEMPERATURE**

**OFFSET TRIMMING AND
STROBE CIRCUIT**

**RESPONSE TIME
FOR 5V STEP AND 5mV OVERDRIVE**


APPLICATIONS INFORMATION

The CMP-01 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-01 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading (C_L). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

the response time will approximate the response time for low values of R_S . It should be noted that the offset nulling terminals do not require bypassing for stability. As with all

MINIMIZING OSCILLATION



MIL-STD-883, METHOD 1015, CONDITION B

The circuit diagram illustrates a digital-to-analog converter (DAC) system. It features a 10-bit D/A converter (DAC100CCQ3) and a 1/2 7474 flip-flop. The DAC is powered by a 15V supply and has a 200Ω resistor connected to its output. The flip-flop is powered by a 15V supply and has its output connected to the DAC input. The DAC output is also connected to a 15V supply through a 1N914 diode. The circuit is labeled with component values and pin numbers.

Key components and connections include:

- 1/2 7474 TYPE "D" FLIP-FLOP:** A 15V supply is connected to pin 3. Pin 1 is connected to ground. Pin 2 is connected to a 1N914 diode. Pin 4 is connected to a 15V supply. Pin 7 is connected to pin 8. Pin 10 is connected to pin 11. Pin 12 is connected to pin 13. Pin 14 is connected to pin 15. Pin 16 is connected to pin 17. Pin 18 is connected to pin 19. Pin 20 is connected to pin 21. Pin 22 is connected to pin 23. Pin 24 is connected to pin 25. Pin 26 is connected to pin 27. Pin 28 is connected to pin 29. Pin 30 is connected to pin 31. Pin 32 is connected to pin 33. Pin 34 is connected to pin 35. Pin 36 is connected to pin 37. Pin 38 is connected to pin 39. Pin 40 is connected to pin 41. Pin 42 is connected to pin 43. Pin 44 is connected to pin 45. Pin 46 is connected to pin 47. Pin 48 is connected to pin 49. Pin 50 is connected to pin 51. Pin 52 is connected to pin 53. Pin 54 is connected to pin 55. Pin 56 is connected to pin 57. Pin 58 is connected to pin 59. Pin 60 is connected to pin 61. Pin 62 is connected to pin 63. Pin 64 is connected to pin 65. Pin 66 is connected to pin 67. Pin 68 is connected to pin 69. Pin 70 is connected to pin 71. Pin 72 is connected to pin 73. Pin 74 is connected to pin 75. Pin 76 is connected to pin 77. Pin 78 is connected to pin 79. Pin 80 is connected to pin 81. Pin 82 is connected to pin 83. Pin 84 is connected to pin 85. Pin 86 is connected to pin 87. Pin 88 is connected to pin 89. Pin 90 is connected to pin 91. Pin 92 is connected to pin 93. Pin 94 is connected to pin 95. Pin 96 is connected to pin 97. Pin 98 is connected to pin 99. Pin 100 is connected to pin 101. Pin 102 is connected to pin 103. Pin 104 is connected to pin 105. Pin 106 is connected to pin 107. Pin 108 is connected to pin 109. Pin 110 is connected to pin 111. Pin 112 is connected to pin 113. Pin 114 is connected to pin 115. Pin 116 is connected to pin 117. Pin 118 is connected to pin 119. Pin 120 is connected to pin 121. Pin 122 is connected to pin 123. Pin 124 is connected to pin 125. Pin 126 is connected to pin 127. Pin 128 is connected to pin 129. Pin 130 is connected to pin 131. Pin 132 is connected to pin 133. Pin 134 is connected to pin 135. Pin 136 is connected to pin 137. Pin 138 is connected to pin 139. Pin 140 is connected to pin 141. Pin 142 is connected to pin 143. Pin 144 is connected to pin 145. Pin 146 is connected to pin 147. Pin 148 is connected to pin 149. Pin 150 is connected to pin 151. Pin 152 is connected to pin 153. Pin 154 is connected to pin 155. Pin 156 is connected to pin 157. Pin 158 is connected to pin 159. Pin 160 is connected to pin 161. Pin 162 is connected to pin 163. Pin 164 is connected to pin 165. Pin 166 is connected to pin 167. Pin 168 is connected to pin 169. Pin 170 is connected to pin 171. Pin 172 is connected to pin 173. Pin 174 is connected to pin 175. Pin 176 is connected to pin 177. Pin 178 is connected to pin 179. Pin 180 is connected to pin 181. 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Pin 422 is connected to pin 423. Pin 424 is connected to pin 425. Pin 426 is connected to pin 427. Pin 428 is connected to pin 429. Pin 430 is connected to pin 431. Pin 432 is connected to pin 433. Pin 434 is connected to pin 435. Pin 436 is connected to pin 437. Pin 438 is connected to pin 439. Pin 440 is connected to pin 441. Pin 442 is connected to pin 443. Pin 444 is connected to pin 445. Pin 446 is connected to pin 447. Pin 448 is connected to pin 449. Pin 450 is connected to pin 451. Pin 452 is connected to pin 453. Pin 454 is connected to pin 455. Pin 456 is connected to pin 457. Pin 458 is connected to pin 459. Pin 460 is connected to pin 461. Pin 462 is connected to pin 463. Pin 464 is connected to pin 465. Pin 466 is connected to pin 467. Pin 468 is connected to pin 469. Pin 470 is connected to pin 471. Pin 472 is connected to pin 473. Pin 474 is connected to pin 475. Pin 476 is connected to pin 477. Pin 478 is connected to pin 479. Pin 480 is connected to pin 481. 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