

# DEVICE ENGINEERING INCORPORATED

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# DEI1066

## OCTAL GND/OPEN INPUT, SERIAL OUTPUT INTERFACE IC

### FEATURES

- Eight GND/OPEN discrete inputs
  - Meet electrical requirements for ABD0100 GND/OPEN discrete input.
  - Hysteresis provides noise immunity
  - Internal pull up resistor with 1mA source current to prevent dry relay contacts.
  - Internal isolation diode
  - Inputs protected from Lightning Induced Transients per DO160D, Section 22, Cat A3 and B3.
- 3-wire serial interface (/CS, CLK, DO)
  - Direct interface to Serial Peripheral Interface (SPI) port.
  - TTL/CMOS compatible inputs and Tristate output
  - 10MHz Data Rate
  - Serial input to expand Shift Register
- Logic Supply Voltage (VCC): 3.3V or 5V
- Analog Supply Voltage (VDD): 5V to 18V
- 16L NB SOIC package
- 16L Ceramic SO Package

### PIN ASSIGNMENTS

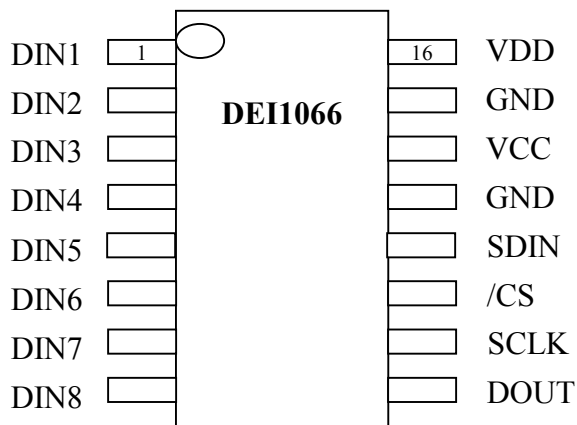


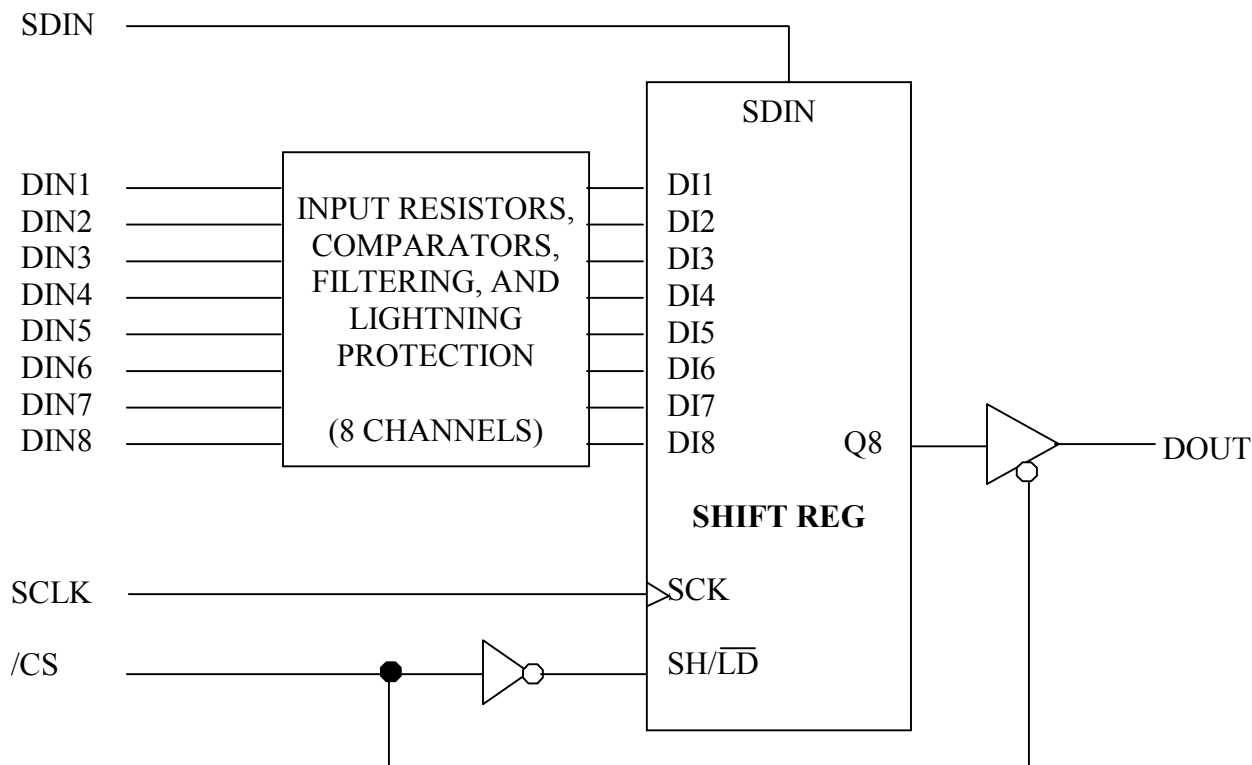
Figure 1 DEI1066 Pin Assignment (16 Lead NB SOIC)

## FUNCTIONAL DESCRIPTION

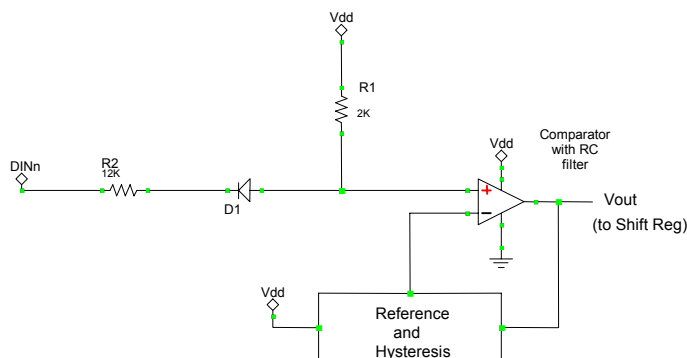
The DEI1066 is an eight-channel discrete-to digital interface BICMOS device. It senses eight Ground/Open format discrete signals of the type commonly found in avionic systems. The data is read from the device via an eight-bit serial shift register with 3-state output. This serial interface is compatible with the industry standard Serial Peripheral Interface (SPI) bus.

**Table 1 Pin Descriptions**

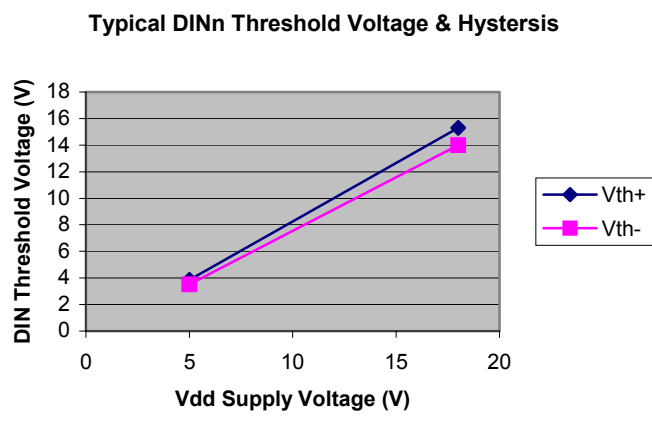
| Pins | Name     | Description                                                                                                                                                                                                                                                                                                                                        |
|------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8-1  | DIN[8:1] | Parallel data inputs. Eight Ground/Open format discrete signals. These have an internal pull-up to VDD. The logic threshold and hysteresis characteristics are determined by the applied VDD voltage.                                                                                                                                              |
| 9    | DOUT     | Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.                                                                                                                                                                                                                                    |
| 10   | SCLK     | Serial Shift Clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and data in stage 8 is shifted out DOUT, being replaced by the data previously stored in stage 7.                                                                                                                          |
| 11   | /CS      | Chip Select. A high-to-low transition on this input loads data from the parallel DIN[8:1] inputs into the shift register. A low level on this input enables the DOUT 3-state output and the shift register. A high level on this input forces DOUT to the high impedance state and disables the shift register so SCLK transitions have no effect. |
| 12   | SDIN     | Serial Data Input. Data on this input is shifted into the shift register on the rising edge of the SCLK input if the /CS input is low. This input has an internal pull-down resistor to GND.                                                                                                                                                       |
| 13   | GND      | Logic Ground.                                                                                                                                                                                                                                                                                                                                      |
| 14   | VCC      | Logic Supply Voltage.                                                                                                                                                                                                                                                                                                                              |
| 15   | GND      | Analog Ground.                                                                                                                                                                                                                                                                                                                                     |
| 16   | VDD      | Analog Supply Voltage.                                                                                                                                                                                                                                                                                                                             |



**Figure 2 DEI1066 LOGIC DIAGRAM**



**Figure 3 DINn Input Circuit**



**Figure 4 DIN Threshold vs Vdd**

**Table 2 Truth Table**

| /CS | SCLK | SDIN | DIN[8:1]                    | SREG Q1   | DOUT             |
|-----|------|------|-----------------------------|-----------|------------------|
| 1   | X    | X    | X                           | X         | HI-Z             |
| ↓   | X    | X    | Sampled into Shift Register | DIN1      | Enabled DIN8     |
| 0   | ↑    | 0    | X                           | 0         | SREG Q8          |
| 0   | ↑    | 1    | X                           | 1         | SREG Q8          |
| 0   | ↓    | X    | X                           | No Change | No Change        |
| ↑   | X    | X    | X                           | No Change | Disabled to HI-Z |

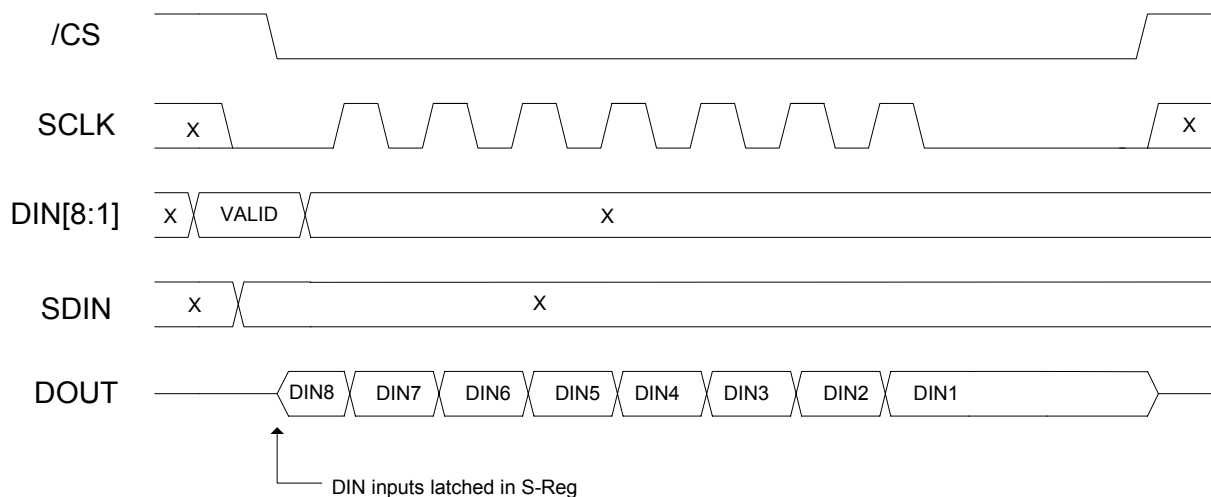
## DIN[8:1] Input Structure

Each of the eight discrete inputs consist of the circuit shown in Figure 3. Each DINn signal is conditioned by the resistor / diode network and presented to the comparator IN+. The reference and hysteresis voltage is developed at the comparator IN-. Some notable features are:

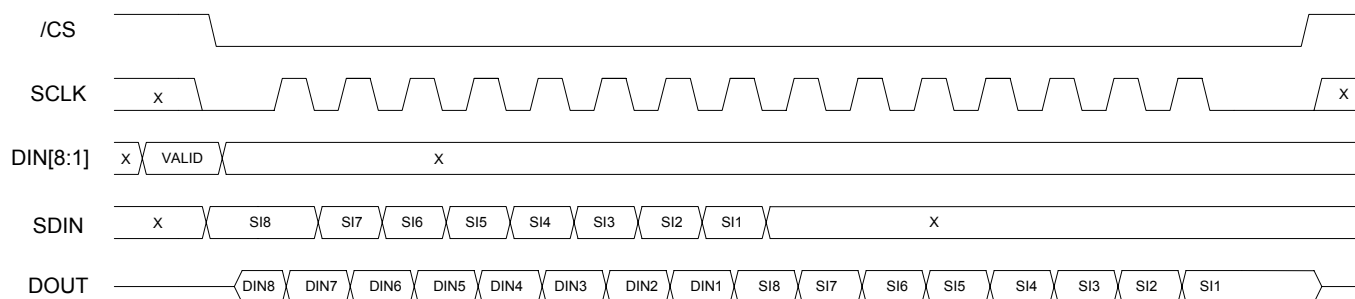
- When Vdd is +15V, the circuit shall source >1mA to a grounded input. This current will prevent a “dry” relay contact.
- The input threshold voltage and hysteresis varies with the Vdd supply.
  - For Vdd of +5V, the falling Vth > 3.5V.
  - For Vdd of +15V, the rising Vth < 14V.
  - For Vdd of +18V, the rising Vth < 15.4V.
  - Hysteresis is approximately as shown in Figure 4.
  - The input thresholds vary with Vdd supply voltages and can be approximated as follows:  
For Vdd = 5V to 18V
    - $V_{lh\_max} = 0.98 \cdot V_{dd} - 0.65V$
    - $V_{hl\_min} = 0.95 \cdot V_{dd} - 0.8V$
- The comparator includes an RC filter to provide noise rejection of transient pulses of up to several uS. Thus there is a relatively large DINx setup time of several uS (Refer to timing parameter tsu2).
- The inputs can withstand continuous input voltages of 40V minimum. The isolation diode breakdown voltage is greater than 50V. The 12K Ohm input resistor is designed to limit diode breakdown current to safe levels during transient events.

## Serial Interface and Shift Register

The DEI1066 digital interface is an 8-Bit Serial or Parallel-Input / Serial-Output Shift Register with 3-State Output. The control inputs to the shift register are connected as shown in Figure 2 DEI1066 LOGIC DIAGRAM to implement an SPI compatible bus consisting of /CS, SCLK, DOUT, and SDIN. The Figure 5 waveform depicts a typical 8-Bit read cycle where the 8 DIN signals are read on to the serial bus. The Figure 6 waveform demonstrates a daisy-chain application where a 16-Bit read cycle includes the serial data passed through from the SDIN input.



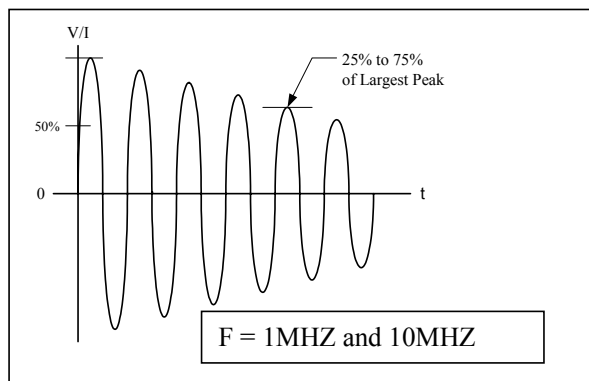
**Figure 5 Serial Bus Read Cycle, 8 Bit**



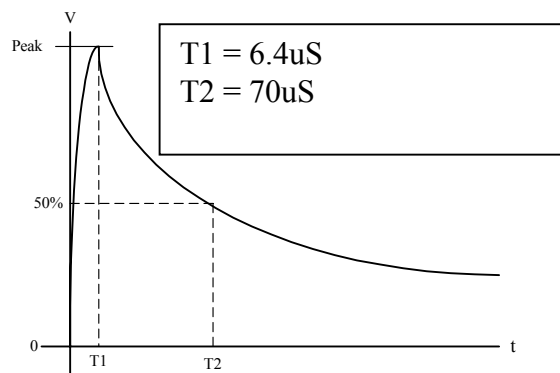
**Figure 6 Serial Bus Read Cycle, 16 Bit Daisy Chain**

## Lightning Protection

DINn inputs are designed to survive lightning induced transients as defined by RTCA DO160D, Section 22, Cat A3 and B3, Waveforms 3, 4, and 5A, Level 3. See waveforms below.



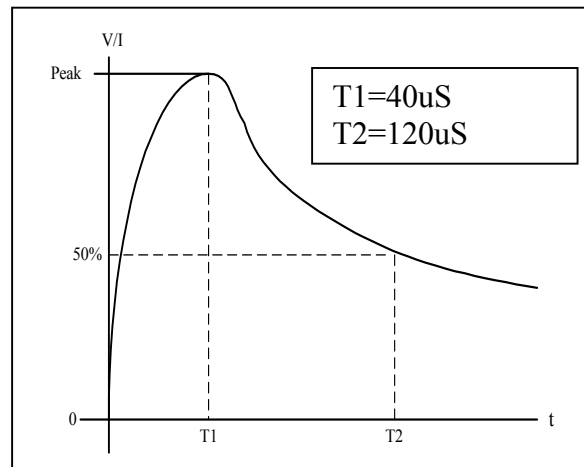
**Figure 7 Voltage / Current Waveform 3**



**Figure 8 Voltage Waveform 4**

Waveform Source Impedance characteristics:

- Waveform 3  $V_{oc}/I_{sc} = 600\text{V} / 24\text{A} \Rightarrow 25 \text{ Ohms}$
- Waveform 4  $V_{oc}/I_{sc} = 300 \text{ V} / 60 \text{ A} \Rightarrow 5 \text{ Ohms}$
- Waveform 5A  $V_{oc} / I_{sc} = 300\text{V} / 300\text{A} \Rightarrow 1 \text{ Ohm}$



**Figure 9 Current/Voltage Waveform 5A**

## ELECTRICAL DESCRIPTION

**Table 3 Absolute Maximum Ratings**

| PARAMETER                                                                            | MIN  | MAX       | UNITS |
|--------------------------------------------------------------------------------------|------|-----------|-------|
| Vcc Supply Voltage                                                                   | -0.3 | +7.0      | V     |
| Vdd Supply Voltage                                                                   | -0.3 | 20        | V     |
| Operating Temperature                                                                |      |           |       |
| Plastic Packages                                                                     | -55  | +85       | °C    |
| Ceramic Packages                                                                     | -55  | +125      |       |
| Storage Temperature                                                                  |      |           |       |
| Plastic Packages                                                                     | -65  | +150      | °C    |
| Ceramic Packages                                                                     | -65  | +150      |       |
| Input Voltage                                                                        |      |           |       |
| DIN[8:1] Continuous                                                                  | -5   | +40       | V     |
| DO160D, Waveform 3, Level 3                                                          | -600 | +600      | V     |
| DO160D, Waveform 4 and 5, Level 3                                                    | -300 | +300      | V     |
| Logic Inputs                                                                         | -1.5 | VCC + 1.5 | V     |
| DOUT                                                                                 | -0.5 | VCC + 0.5 | V     |
| Power Dissipation @ 85 °C: (> 10 Sec)                                                |      |           |       |
| 16 Lead SOIC                                                                         |      | 0.8       | W     |
| 16 Lead CSOP                                                                         |      | 0.53      | W     |
| Junction Temperature:                                                                |      |           |       |
| Tjmax, Plastic Packages                                                              |      | 145       | °C    |
| Tjmax, Ceramic Packages                                                              |      | 150       | °C    |
| ESD per JEDEC A114-A Human Body Model                                                |      |           |       |
| Logic and Supply pins                                                                |      | 2000      | V     |
| DIN pins                                                                             |      | 1000      |       |
| Peak Body Temperature                                                                |      |           |       |
| Non-G Plastic Packages                                                               |      | 240       | °C    |
| - G Plastic Packages                                                                 |      | 260       |       |
| Ceramic Packages                                                                     |      | 240       |       |
| <b>Notes:</b>                                                                        |      |           |       |
| 1. Stresses above absolute maximum ratings may cause permanent damage to the device. |      |           |       |
| 2. Voltages referenced to Ground                                                     |      |           |       |

**Table 4 Recommended Operating Conditions**

| PARAMETER                | SYMBOL     | CONDITIONS                       |
|--------------------------|------------|----------------------------------|
| Supply Voltage           | VCC<br>VDD | 5.0V±10%, 3.3V±10%<br>5.0 to 18V |
| Logic Inputs and Outputs |            | 0 to VCC                         |
| Discrete Inputs          | DIN[8:1]   | 0 to 40V                         |
| Operating Temperature    |            |                                  |
| Plastic                  |            | -55 to +85 °C                    |
| Ceramic                  |            | -55 to +125 °C                   |

**Table 5 DC Electrical Characteristics**

| SYMBOL                                        | PARAMETER                                              | TEST CONDITIONS                            | VCC (V)           | LIMITS            |                   | UNIT |
|-----------------------------------------------|--------------------------------------------------------|--------------------------------------------|-------------------|-------------------|-------------------|------|
|                                               |                                                        |                                            |                   | -55 to +85°C      | -55 to +125°C     |      |
| LOGIC INPUTS AND OUTPUTS<br>VDD = +5V to +18V |                                                        |                                            |                   |                   |                   |      |
| V <sub>IH</sub>                               | Min hi level input voltage                             |                                            | 3.0<br>4.5<br>5.5 | 2.0<br>2.0<br>2.0 | 2.0<br>2.0<br>2.0 | V    |
| V <sub>IL</sub>                               | Max lo level input voltage                             |                                            | 3.0<br>4.5<br>5.5 | 0.8<br>0.8<br>0.8 | 0.8<br>0.8<br>0.8 | V    |
| V <sub>Ihst</sub>                             | Min input hysteresis voltage,<br>SCLK input            | (1)                                        | 3.0<br>4.5<br>5.5 | 50                | 50                | mV   |
| V <sub>OH</sub>                               | Min hi level output voltage                            | I <sub>OUT</sub>   < 20uA                  | 3.0<br>4.5<br>5.5 | VCC – 0.1         | VCC – 0.1         | V    |
|                                               |                                                        | I <sub>OUT</sub>   < 4.5mA                 | 4.5<br>5.5        | 3.2<br>4.5        | 3.0<br>4.3        | V    |
| V <sub>OL</sub>                               | Max low level output voltage                           | I <sub>OUT</sub>   < 20uA                  | 3.0<br>4.5<br>5.5 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V    |
|                                               |                                                        | I <sub>OUT</sub>   < 4.5mA                 | 4.5<br>5.5        | 0.33<br>0.33      | 0.40<br>0.40      | V    |
| I <sub>IN</sub>                               | Max input leakage<br>Logic inputs except SDIN.<br>SDIN | Vin = Vcc or GND                           | 5.5<br>5.5        | ±1.0<br>±750      | ±2.0<br>±750      | uA   |
| I <sub>OZ</sub>                               | Max 3-state leakage current                            | Output in Hi Impedance state.              | 5.5               | ±5.0              | ±10.0             | uA   |
| DISCRETE INPUTS<br>VDD = +18V                 |                                                        |                                            |                   |                   |                   |      |
| V <sub>IH</sub>                               | Min HI level input voltage                             |                                            | 3.0 to 5.5        | 15.7              | 15.9              | V    |
| V <sub>IL</sub>                               | Max LO level input voltage                             |                                            | 3.0 to 5.5        | 14.2              | 14.2              | V    |
| V <sub>Ihst</sub>                             | Min input hysteresis voltage                           |                                            | 3.0 to 5.5        | 1.0               | 1.0               | V    |
| I <sub>IH</sub>                               | Max hi level input current                             | Vin = 18V<br>Vin = 40V                     | 3.0 to 5.5        | 5<br>20           | 10<br>40          | uA   |
| I <sub>ILmax</sub>                            | Max lo level input current                             | Vin = 0V                                   | 3.0 to 5.5        | -1.6              | -1.6              | mA   |
| I <sub>ILmin</sub>                            | Min lo level input current                             | Vin = 0V                                   | 3.0 to 5.5        | -1.0              | -1.0              | mA   |
| DISCRETE INPUTS<br>VDD = +5V                  |                                                        |                                            |                   |                   |                   |      |
| V <sub>IH</sub>                               | Min HI level input voltage                             |                                            | 3.0 to 5.5        | 4.35              | 4.35              | V    |
| V <sub>IL</sub>                               | Max LO level input voltage                             |                                            | 3.0 to 5.5        | 3.53              | 3.53              | V    |
| V <sub>Ihst</sub>                             | Min input hysteresis voltage                           |                                            | 3.0 to 5.5        | 0.33              | 0.33              | V    |
| I <sub>IH</sub>                               | Max hi level input current                             | Vin = 18V<br>Vin = 40V                     | 3.0 to 5.5        | 5<br>20           | 10<br>40          | uA   |
| I <sub>ILmax</sub>                            | Max lo level input current                             | Vin = 0V                                   | 3.0 to 5.5        | -0.5              | -0.5              | mA   |
| I <sub>ILmin</sub>                            | Min lo level input current                             | Vin = 0V                                   | 3.0 to 5.5        | -0.25             | -0.25             | mA   |
| SUPPLY VOLTAGES<br>VDD = +15V                 |                                                        |                                            |                   |                   |                   |      |
| ICC                                           | Max quiescent logic supply current                     | Vin(logic) = Vcc or GND<br>VIN[8:1] = open | 6.0               | 200               | 400               | uA   |
| IDD                                           | Max quiescent analog supply current                    | Vin(logic) = Vcc or GND<br>VIN[8:1] = Open | 6.0               | 11                | 11                | mA   |
|                                               |                                                        | VIN[8:1] = GND                             | 6.0               | 23                | 24                |      |

**Table 6 AC Electrical Characteristics**

| SYMBOL           | PARAMETER<br>(4,6 & 7)                                                                             | VCC<br>(V) | LIMITS          |                  | UNIT |
|------------------|----------------------------------------------------------------------------------------------------|------------|-----------------|------------------|------|
|                  |                                                                                                    |            | -55 to<br>+85°C | -55 to<br>+125°C |      |
| f <sub>MAX</sub> | Maximum SCLK frequency. (50% duty cycle) (5)<br><br>Maximum usable SCLK frequency = 1/(tp2 + tsu3) | 2.0        | 4.8             | 4.0              | MHz  |
|                  |                                                                                                    | 4.5        | 24              | 20               |      |
|                  |                                                                                                    | 6.0        | 28              | 24               |      |
|                  |                                                                                                    | 2.0        | 2.8             | 2.2              |      |
|                  |                                                                                                    | 4.5        | 10.7            | 8.2              |      |
|                  |                                                                                                    | 6.0        | 14.6            | 11.2             |      |
| t <sub>w</sub>   | Minimum SCLK pulse width. (50% duty cycle)                                                         | 2.0        | 100             | 120              | ns   |
|                  |                                                                                                    | 4.5        | 20              | 24               |      |
|                  |                                                                                                    | 6.0        | 17              | 20               |      |
| t <sub>su1</sub> | Minimum setup time, SCLK low to /CS↓.                                                              | 2.0        | 100             | 100              | ns   |
|                  |                                                                                                    | 4.5        | 50              | 50               |      |
|                  |                                                                                                    | 6.0        | 40              | 40               |      |
| t <sub>h1</sub>  | Minimum hold time, /CS↓ to SCLK↑.                                                                  | 2.0        | 20              | 20               | ns   |
|                  |                                                                                                    | 4.5        | 20              | 20               |      |
|                  |                                                                                                    | 6.0        | 20              | 20               |      |
| t <sub>su2</sub> | Setup time, DIN valid to /CS↓. (8)                                                                 | 5.0        | 35              | 35               | us   |
| t <sub>h2</sub>  | Hold time, /CS↓ to DIN not valid. (8)                                                              | 5.0        | -1.5            | -1.5             | us   |
| t <sub>su3</sub> | Minimum setup time, SDIN valid to SCLK↑.                                                           | 2.0        | 75              | 80               | ns   |
|                  |                                                                                                    | 4.5        | 20              | 25               |      |
|                  |                                                                                                    | 6.0        | 15              | 15               |      |
| t <sub>h3</sub>  | Minimum hold time, SCLK↑ to SDIN not valid.                                                        | 2.0        | 5               | 5                | ns   |
|                  |                                                                                                    | 4.5        | 5               | 5                |      |
|                  |                                                                                                    | 6.0        | 5               | 5                |      |
| t <sub>p1</sub>  | Maximum propagation delay, /CS↓ to DOUT valid. (1)                                                 | 2.0        | 220             | 265              | ns   |
|                  |                                                                                                    | 4.5        | 55              | 72               |      |
|                  |                                                                                                    | 6.0        | 47              | 52               |      |
| t <sub>p2</sub>  | Maximum propagation delay, SCLK↑ to DOUT valid. (1)                                                | 2.0        | 295             | 380              | ns   |
|                  |                                                                                                    | 4.5        | 90              | 102              |      |
|                  |                                                                                                    | 6.0        | 70              | 75               |      |
| t <sub>p3</sub>  | Maximum propagation delay, /CS↑ to DOUT HI-Z. (1) (2) (3)                                          | 2.0        | 320             | 380              | ns   |
|                  |                                                                                                    | 4.5        | 80              | 103              |      |
|                  |                                                                                                    | 6.0        | 59              | 77               |      |
| t <sub>p4</sub>  | Minimum time between /CS active.                                                                   | 2.0        | 50              | 50               | ns   |
|                  |                                                                                                    | 4.5        | 25              | 25               |      |
|                  |                                                                                                    | 6.0        | 25              | 25               |      |
| C <sub>in</sub>  | Maximum logic input pin Capacitance. (5)                                                           |            | 10              | 10               | pF   |
| C <sub>out</sub> | Maximum DOUT pin capacitance, output in HI-Z state. (5)                                            |            | 15              | 15               | pF   |

1. DOUT loaded with 50pF to GND.
2. DOUT loaded with 1K Ohms to GND for Hi output, 1K Ohms to VCC for Low output.
3. Timing measured at 25%VCC for “0” to Hi-Z, 75%VCC for “1” to Hi-Z.
4. Sample tested on lot basis.
5. Not tested
6. Unless otherwise noted, VDD=+15V, VIL = 0V, VIH = VCC
7. Measurements made at 50%VCC.
8. Vdd = 6V. t<sub>su2</sub> represents the maximum possible propagation delay through the input comparator. t<sub>h2</sub> represents the minimum possible propagation delay through the input comparator. The negative hold time denotes that DIN may change prior to /CS↓ and still be valid data at the S-Register.

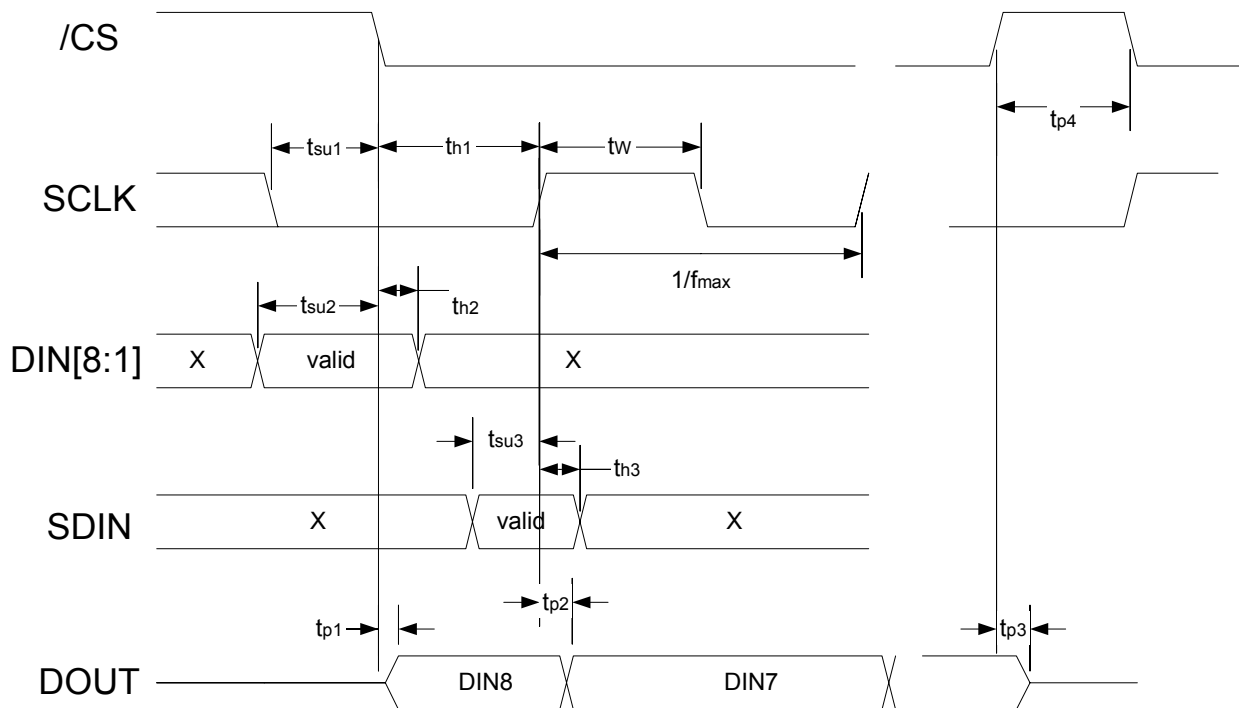


Figure 10 Switching Waveforms

| Table 7: Package Characteristics              |                          |                                 |                     |
|-----------------------------------------------|--------------------------|---------------------------------|---------------------|
| PACKAGE TYPE                                  | 16 Lead SOIC Narrow Body | 16 Lead SOIC Narrow Body, Green | 16 Lead Ceramic SOP |
| REFERENCE                                     | 16L SOIC NB              | 16L SOIC NB G                   | 16L CSOP            |
| <b>THERMAL RESISTANCE:</b>                    |                          |                                 |                     |
| $\theta_{JA}$ (4 layer PCB with Power Planes) | ~74 °C/W                 | ~74 °C/W                        | -                   |
| $\theta_{JC}$                                 | ~30 °C/W                 | ~30 °C/W                        | 23 °C/W             |
| JEDEC MOISTURE SENSITIVITY LEVEL (MSL)        | MSL 2 / 240°C            | MSL 1 / 260°C                   | Hermetic            |
| LEAD FINISH MATERIAL / JEDEC Pb-free CODE     | SnPb                     | NiPdAu e4                       | Au e4               |
| Pb-Free DESIGNATION                           | Not Pb-free              | RoHS Compliant                  | Pb Free             |
| JEDEC REFERENCE                               | MS-012-AC                | MS-012-AC                       | -                   |

## PACKAGE DESCRIPTIONS

### 16 Lead Narrow Body SOIC – Non-G Package

Moisture Sensitivity:

Level 2 per JEDEC J-STD-020A (1yr floor life) (Non – G Package)

$\Theta_{ja}$ :

$\sim 73^{\circ}\text{C/W}$  (Mounted on 4 layer PCB)

$\Theta_{jc}$ :

$\sim 29^{\circ}\text{C/W}$

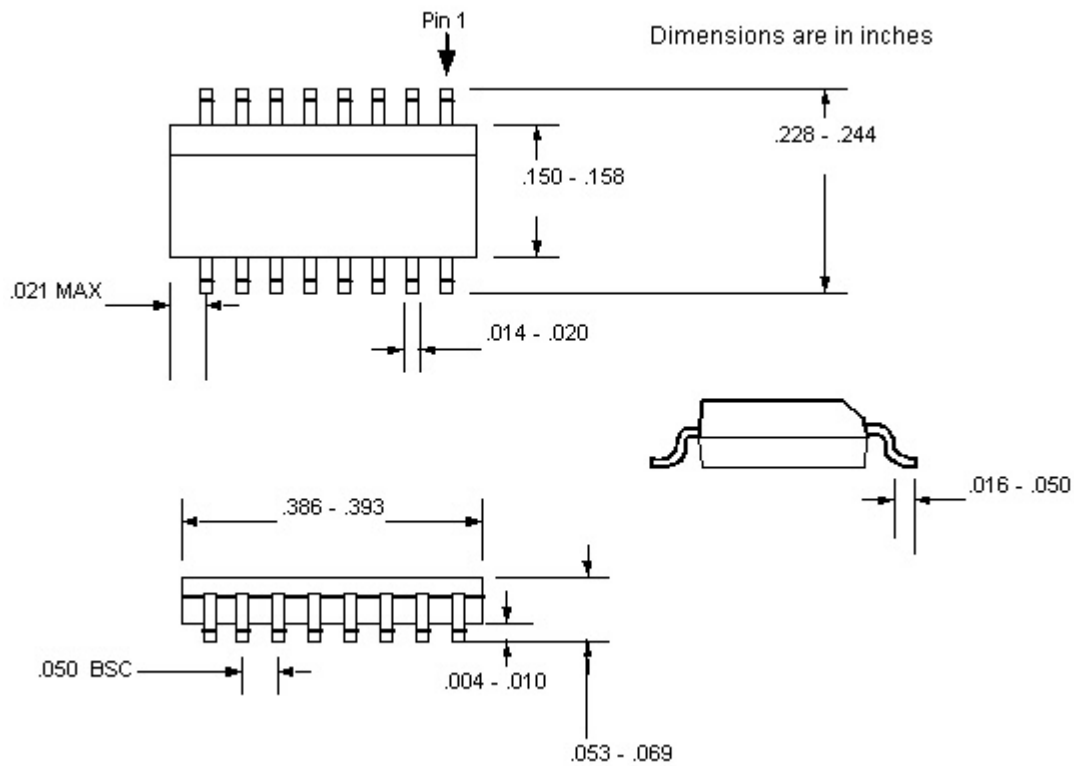


Figure 11. Mechanical Outline - 16 Lead Narrow Body SOIC Non – G Package

## 16 Lead Narrow Body SOIC -G Package

Moisture Sensitivity:

Level 1 per JEDEC J-STD-020A (1yr floor life) (Non – G Package)

$\Theta_{ja}$ :

$\sim 73^{\circ}\text{C/W}$  (Mounted on 4 layer PCB)

$\Theta_{jc}$ :

$\sim 29^{\circ}\text{C/W}$

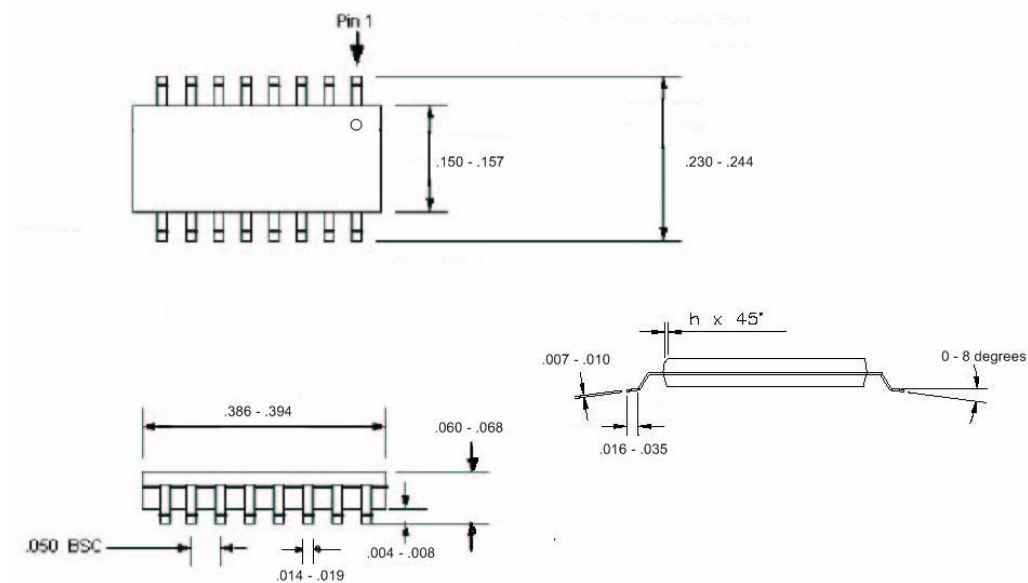


Figure 12 Mechanical Outline - 16 Lead Narrow Body SOIC - G Package

## 16 Lead Ceramic Small Outline Package (CSOP)

Theta ja: 122 C/W Device mounted on 2 layer PCB  
 Theta jc: 5 C/W  
 Moisture Sensitivity Level: Hermetic

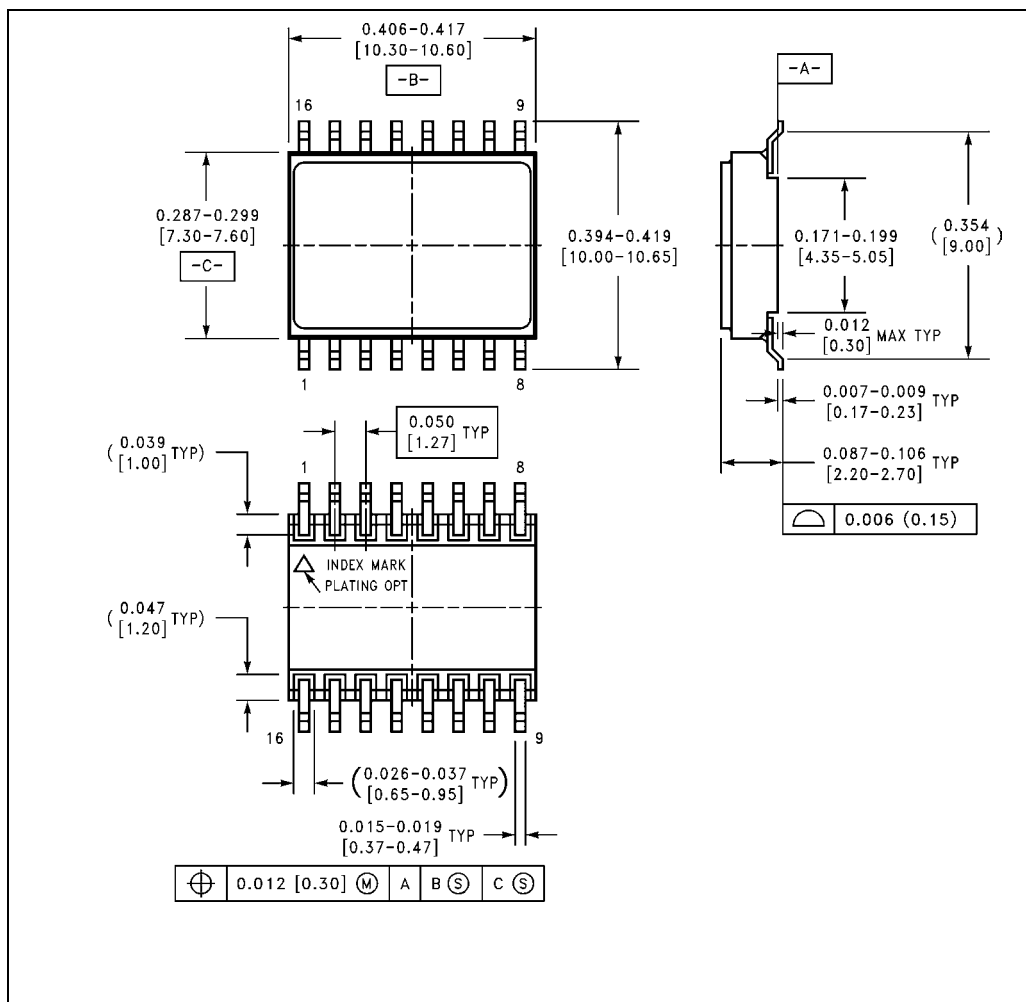


Figure 13 16 Lead CSOP Outline Drawing

## ORDERING INFORMATION

Table 8

| Part Number   | Marking             | Package      | Burn In        | Temperature   |
|---------------|---------------------|--------------|----------------|---------------|
| DEI1066-SES   | DEI1066-SES         | 16 SOIC NB   | No             | -55 / +85 °C  |
| DEI1066-SES-G | DEI1066-SES-G<br>E4 | 16 SOIC NB G | No             | -55 / +85 °C  |
| DEI1066-SMS-G | DEI1066-SMS-G<br>E4 | 16 SOIC NB G | No             | -55 / +125 °C |
| DEI1066-SMB-G | DEI1066-SMB-G<br>E4 | 16 SOIC NB G | 96hr / +125 °C | -55 / +125 °C |
| DEI1066-WMS   | DEI1066-WMS         | 16 CSOP      | No             | -55 / +125 °C |
| DEI1066-WMB   | DEI1066-WMB         | 16 CSOP      | 96hr / +125 °C | -55 / +125 °C |

DEI reserves the right to make changes to any products or specifications herein. DEI makes no warranty, representation, or guarantee regarding suitability of its products for any particular purpose.