FAIRCHILD SEMICONDUCTOR™

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FIN1028
3.3V LVDS 2-Bit High Speed Differential Receiver

General Description

This dual receiver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100 mV, to LVTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1028 can be paired with its companion driver, the FIN1027, or any other LVDS driver.

Features

- Greater than 400Mbs data rate
- 3.3V power supply operation
- 0.4ns maximum differential pulse skew
- 2.5ns maximum propagation delay
- Low power dissipation
- Power-Off protection
- Fail safe protection for open-circuit, shorted and terminated conditions
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Flow-through pinout simplifies PCB layout
- 8-Lead SOIC and 8-terminal MLP packages save space

Ordering Code:

Order Number	Package Number	Package Description
FIN1028M (Note 1)	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1028MPX (Preliminary)	MLP08C	8-Terminal Molded Leadless Package (MLP) Dual, JEDEC MO-229, 2mm Square [TAPE and REEL]

Note 1: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Pin Descriptions

Pin Name	Description
R_{OUT1}, R_{OUT2}	LVTTL Data Outputs
R_{IN1+}, R_{IN2+}	Non-inverting LVDS Inputs
R_{IN1-}, R_{IN2-}	Inverting LVDS Inputs
V_{CC}	Power Supply
GND	Ground

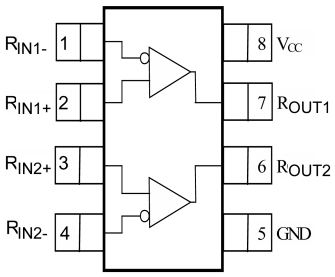
Function Table

Input	Outputs	
R_{IN+}	R_{IN+}	R_{OUT}
L	H	L
H	L	H
Fail Safe Condition		H

H = HIGH Logic Level
L = LOW Logic Level
Fail Safe = Open, Shorted, Terminated

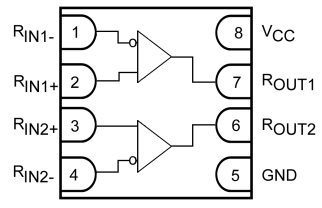
Connection Diagrams

Pin Assignment for SOIC



(Top View)

Terminal Assignments for MLP



(Top Through View)

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (R_{INx+}, R_{INx-})	−0.5V to +4.7V
DC Output Voltage (R_{OUTx})	−0.5V to +6V
DC Output Current (I_O)	16 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
ESD (Human Body Model)	≥ 6500V
ESD (Machine Model)	≥ 300V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Input Voltage (V_{IN})	0 to V_{CC}
Magnitude of Differential Voltage ($\|V_{ID}\|$)	100 mV to V_{CC}
Common-mode Input Voltage (V_{IC})	0.05V to 2.35V
Operating Temperature (T_A)	−40°C to +85°C

Note 2: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
V_{TH}	Differential Input Threshold HIGH	See Figure 1 and Table 1			100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 1 and Table 1	−100			mV
I_{IN}	Input Current	V_{IN} = 0V or V_{CC}			±20	µA
$I_{I(OFF)}$	Power-OFF Input Current	V_{CC} = 0V, V_{IN} = 0V or 3.6V			±20	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −100 µA	V_{CC} −0.2			V
		I_{OH} = −8 mA	2.4			
V_{OL}	Output LOW Voltage	I_{OH} = 100 µA			0.2	V
		I_{OL} = 8 mA			0.5	
V_{IK}	Input Clamp Voltage	I_{IK} = −18 mA	−1.5			V
I_{CC}	Power Supply Current	(R_{IN+} = 1V and R_{IN-} = 1.4V) or (R_{IN+} = 1.4V and R_{IN-} = 1V)			9	mA
C_{IN}	Input Capacitance			4		pF
C_{OUT}	Output Capacitance			6		pF

Note 3: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

AC Electrical Characteristics

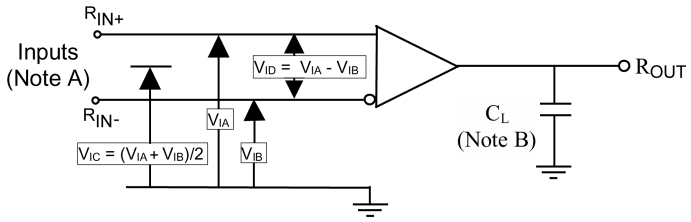
Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 4)	Max	Units
t_{PLH}	Differential Propagation Delay LOW-to-HIGH	$\|V_{ID}\|$ = 400 mV, C_L = 10 pF, See Figure 1 and Figure 2	0.9		2.5	ns
t_{PHL}	Differential Propagation Delay HIGH-to-LOW		0.9		2.5	ns
t_{TLH}	Output Rise Time (20% to 80%)			0.5		ns
t_{THL}	Output Fall Time (80% to 20%)			0.5		ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} - t_{PHL}\|$				0.4	ns
$t_{SK(LH)}$, $t_{SK(HL)}$	Channel-to-Channel Skew (Note 5)				0.3	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 6)				1.0	ns

Note 4: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

Note 5: $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

Note 6: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.



Note A: All input pulses have frequency = 10 MHz, t_R or t_F = 1 ns
Note B: C_L includes all probe and fixture capacitances

FIGURE 1. Differential Driver Propagation Delay and Transition Time Test Circuit

TABLE 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	–100	1.2
2.4	2.3	100	2.35
2.3	2.4	–100	2.35
0.1	0	100	0.05
0	0.1	–100	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3

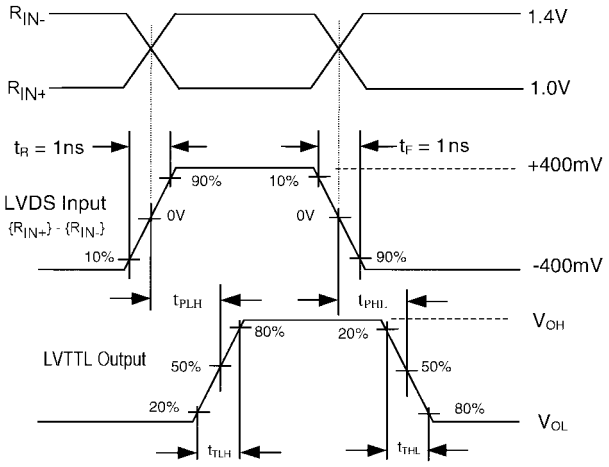


FIGURE 2. AC Waveforms

DC /AC Typical Performance Curves

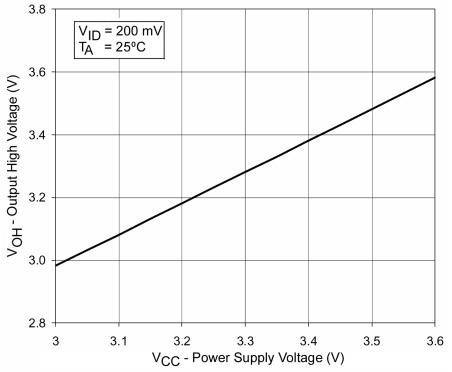


FIGURE 3. Output High Voltage vs. Power Supply Voltage

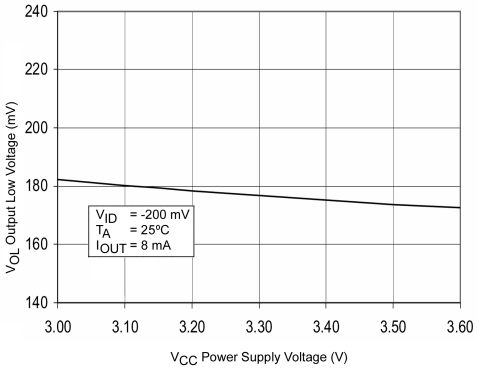


FIGURE 4. Output Low Voltage vs. Power Supply Voltage

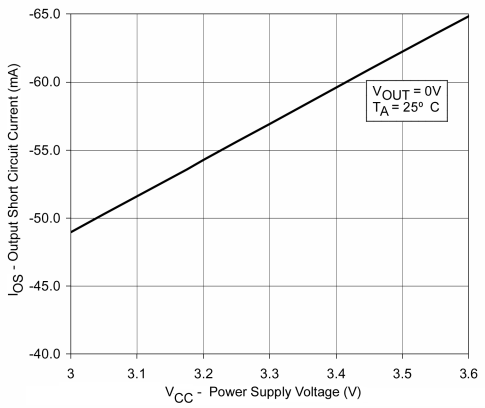


FIGURE 5. Output Short Circuit Current vs. Power Supply Voltage

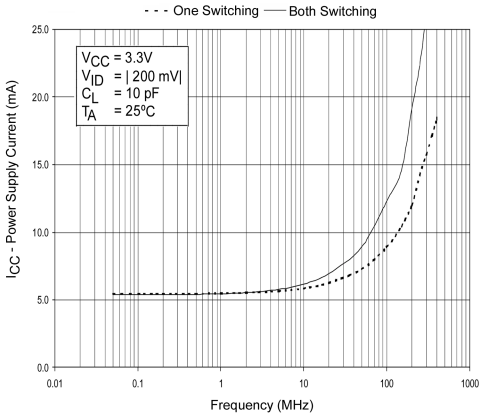


FIGURE 6. Power Supply Current vs. Frequency

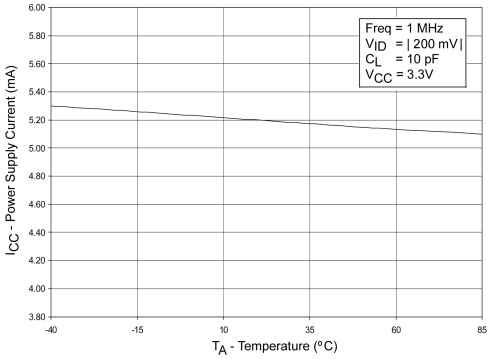


FIGURE 7. Power Supply Current vs. Ambient Temperature

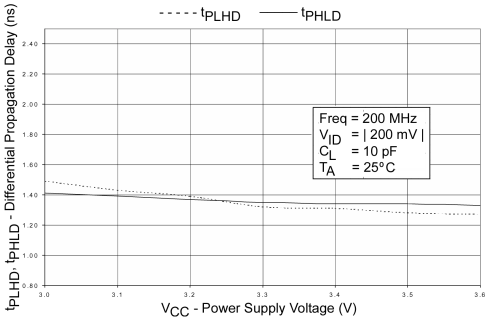


FIGURE 8. Differential Propagation Delay vs. Power Supply Voltage

DC /AC Typical Performance Curves (Continued)

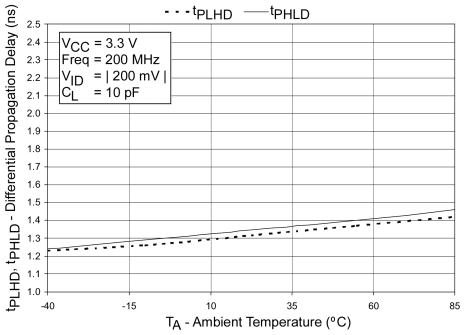


FIGURE 9. Differential Propagation Delay vs. Ambient Temperature

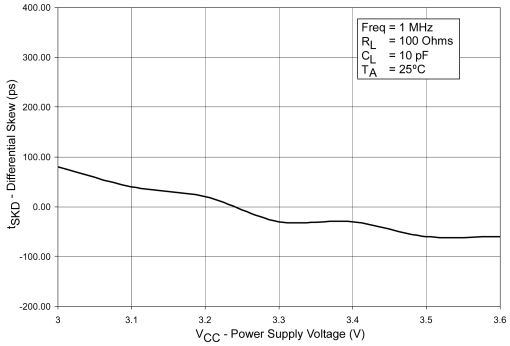


FIGURE 10. Differential Skew (t_{PLH} - t_{PHL}) vs. Power Supply Voltage

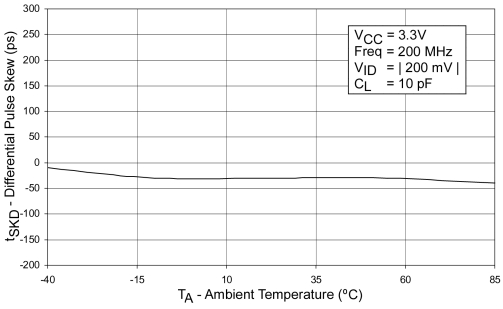


FIGURE 11. Differential Skew (t_{PHL} - t_{PHL}) vs. Ambient Temperature

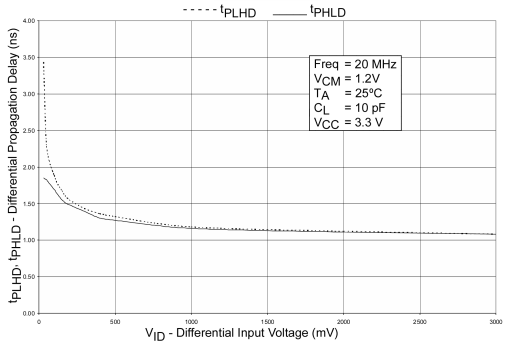


FIGURE 12. Differential Propagation Delay vs. Differential Input Voltage

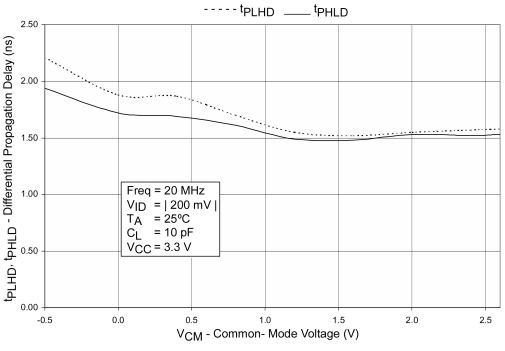


FIGURE 13. Differential Propagation Delay vs. Common-Mode Voltage

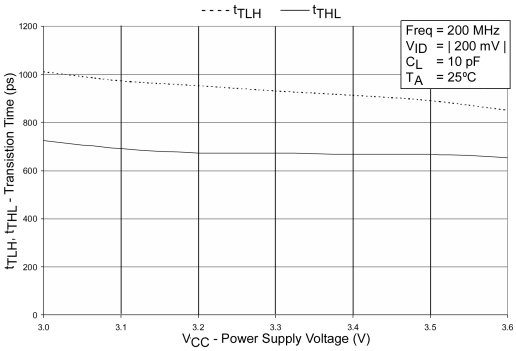


FIGURE 14. Transition Time vs. Power Supply Voltage

DC /AC Typical Performance Curves (Continued)

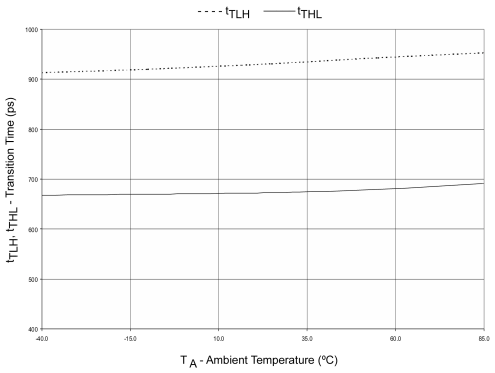


FIGURE 15. Transition Time vs. Ambient Temperature

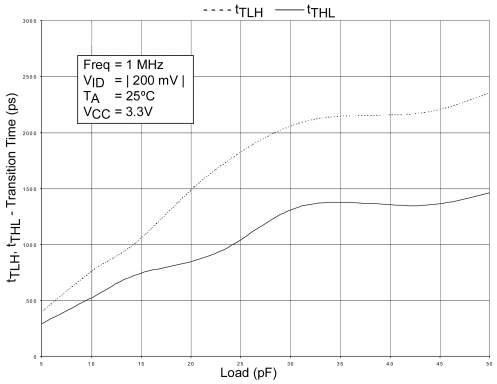


FIGURE 16. Differential Propagation Delay vs. Load

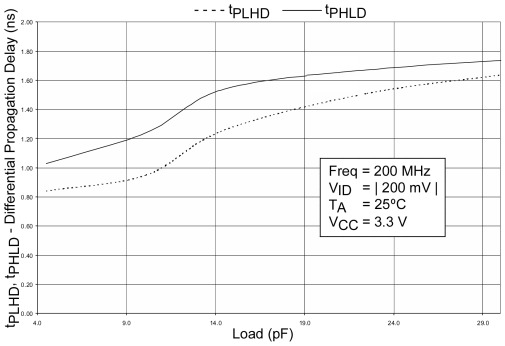


FIGURE 17. Differential Propagation Delay vs. Load

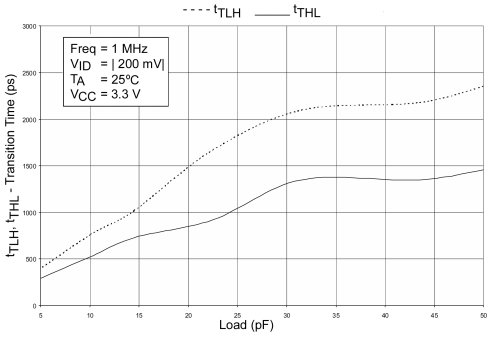


FIGURE 18. Transition Time vs. Load

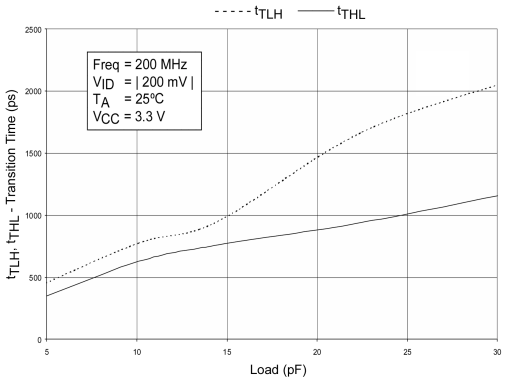


FIGURE 19. Transition Time vs. Load

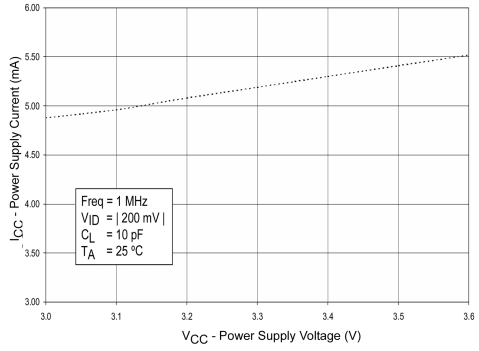


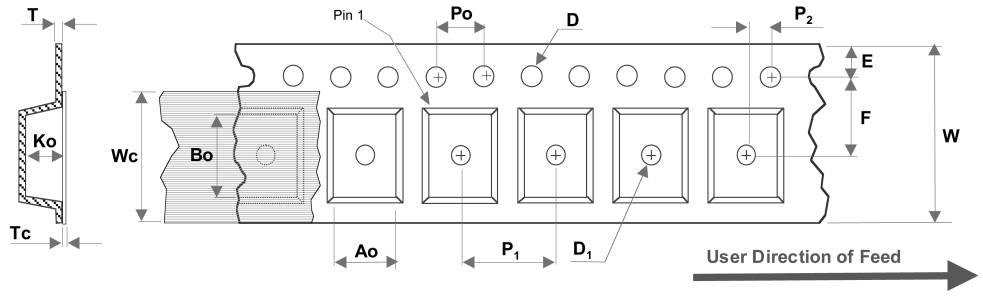
FIGURE 20. Power Supply Current vs. Power Supply Voltage

Tape and Reel Specification

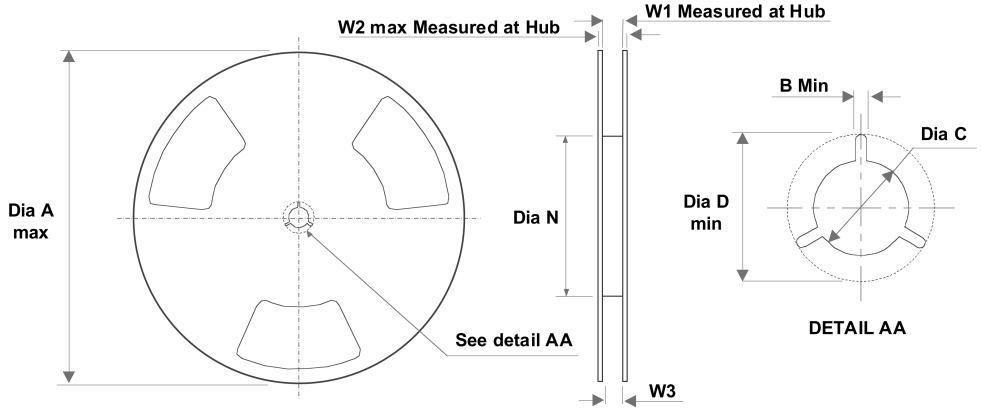
TAPE FORMAT for MLP

Package	Ao ±0.10	Bo ±0.10	D ±0.05	D_1 Min	E ±0.1	F ±0.1	Ko ±0.1	P_1 TYP	Po TYP	P_2 ±0/05	T TYP	T_C ±0.005	W ±0.3	Wc TYP
2 x 2	2.30	2.30	1.55	1.0	1.75	3.5	1.0	8.0	4.0	2.0	0.3	0.06	8.0	5.3

MLP Embossed Tape Dimensions (Dimensions are in millimeters)

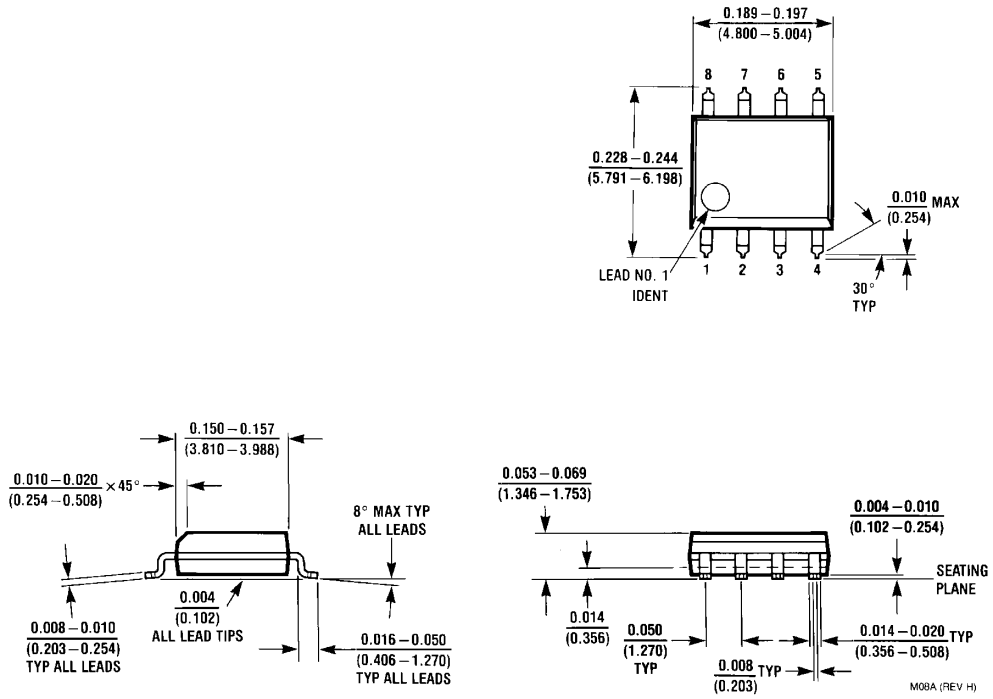


REEL DIMENSIONS (millimeters)



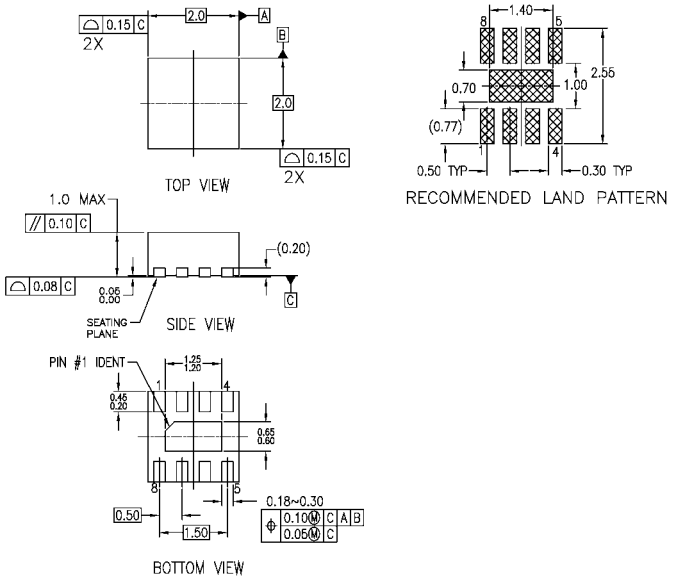
Tape Width	Dia A Max	Dim B Min	Dia C +0.5/–0.2	Dia D Min	Dim N Min	Dim W1 +2/–0	Dim W2 Max	Dim W3 (LSL - USL)
8 mm	330	1.5	13	20.2	178	8.4	14.4	7.9 ~ 10.4

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCD-3, DATED 11/2001
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP08CrevB

8-Terminal Molded Leadless Package (MLP) Dual, JEDEC MO-229, 2mm Square
Package Number MLP08C
(Preliminary)