

Silicon NPN Power Transistors

BU102

DESCRIPTION

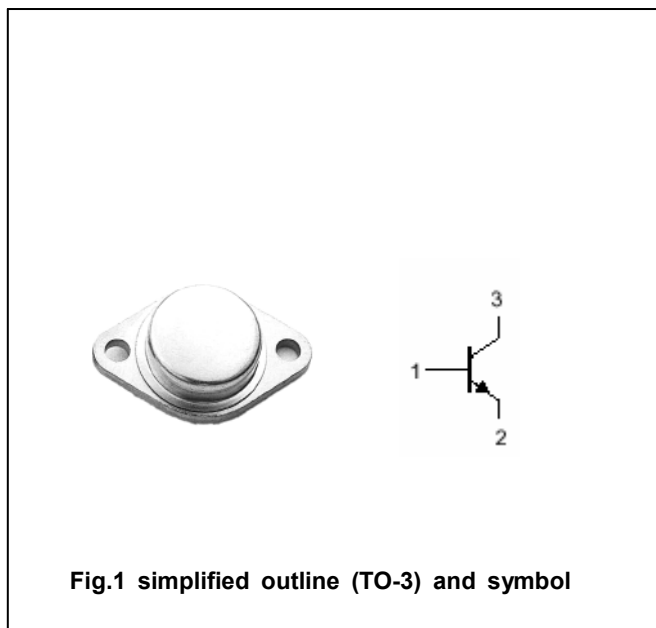
- With TO-3 package
- $V_{CEO(sus)}=150V$ (min)

APPLICATIONS

- Designed for horizontal deflection output stage of CTV receivers

PINNING(see fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

**Absolute maximum ratings($T_a=\square$)**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	400	V
V_{CEO}	Collector-emitter voltage	Open base	150	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		7	A
P_C	Collector power dissipation	$T_C=25\square$	100	W
T_j	Junction temperature		150	$\square$
T_{stg}	Storage temperature		-55~150	$\square$

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CHARACTERISTICS

Tj=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CEO(SUS)}$	Collector-emitter sustaining voltage	$I_C=100mA; I_B=0$	150			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	$I_E=1mA; I_C=0$	6			V
$V_{(BR)CBO}$	Collector-base breakdown voltage	$I_C=1mA; I_E=0$	400			V
V_{CEsat}	Collector-emitter saturation voltage	$I_C=5A; I_B=1.0A$			2.0	V
V_{BEsat}	Base-emitter saturation voltage	$I_C=5A; I_B=1.0A$			2.5	V
I_{CBO}	Collector cut-off current	$V_{CB}=400V; I_E=0$			0.1	mA
I_{CEO}	Collector cut-off current	$V_{CE}=100V; I_E=0$			1.0	mA
I_{EBO}	Emitter cut-off current	$V_{EB}=5V; I_C=0$			0.1	mA
h_{FE}	DC current gain	$I_C=1A; V_{CE}=5V$	30		120	

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PACKAGE OUTLINE

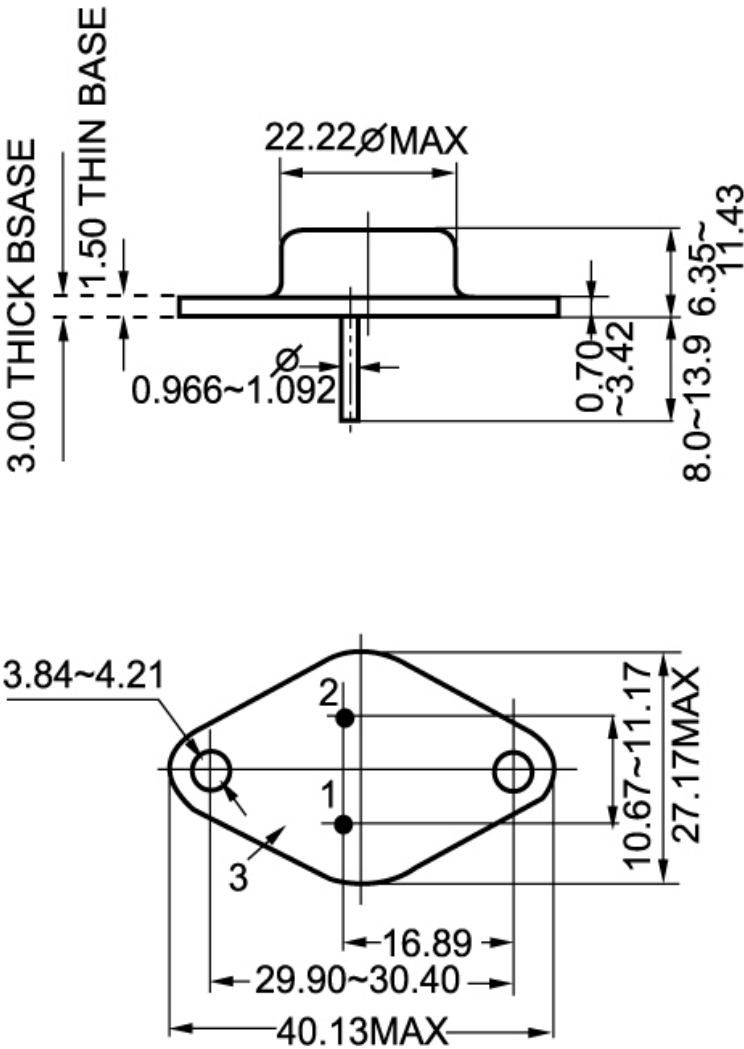


Fig.2 Outline dimensions