

74AC373, 74ACT373

Octal Transparent Latch with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Eight latches in a single package
- 3-STATE outputs for bus interfacing
- Outputs source/sink 24mA
- ACT373 has TTL-compatible inputs

General Description

The AC/ACT373 consists of eight latches with 3-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high impedance state.

Ordering Information

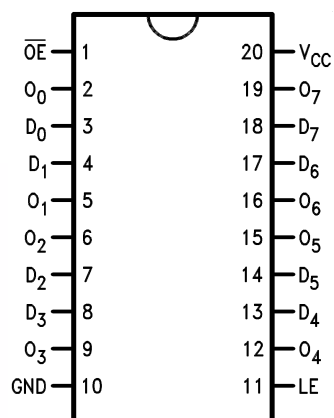
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74AC373SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74AC373SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC373MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC373PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74ACT373SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74ACT373SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ACT373MSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide |
| 74ACT373MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT373PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



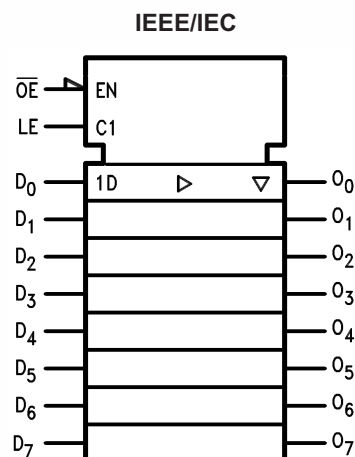
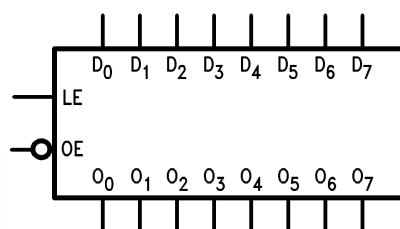
Pin Description

| Pin Names | Description |
|--------------------------------|-----------------------|
| D ₀ –D ₇ | Data Inputs |
| LE | Latch Enable Input |
| OE | Output Enable Input |
| O ₀ –O ₇ | 3-STATE Latch Outputs |

Functional Description

The AC/ACT373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D-type input changes. When LE is LOW, the latches store the information that was present on the D-type inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Symbols



Truth Table

| Inputs | | | Outputs |
|--------|-----------------|----------------|----------------|
| LE | \overline{OE} | D _n | O _n |
| X | H | X | Z |
| H | L | L | L |
| H | L | H | H |
| L | L | X | O ₀ |

H = HIGH Voltage Level

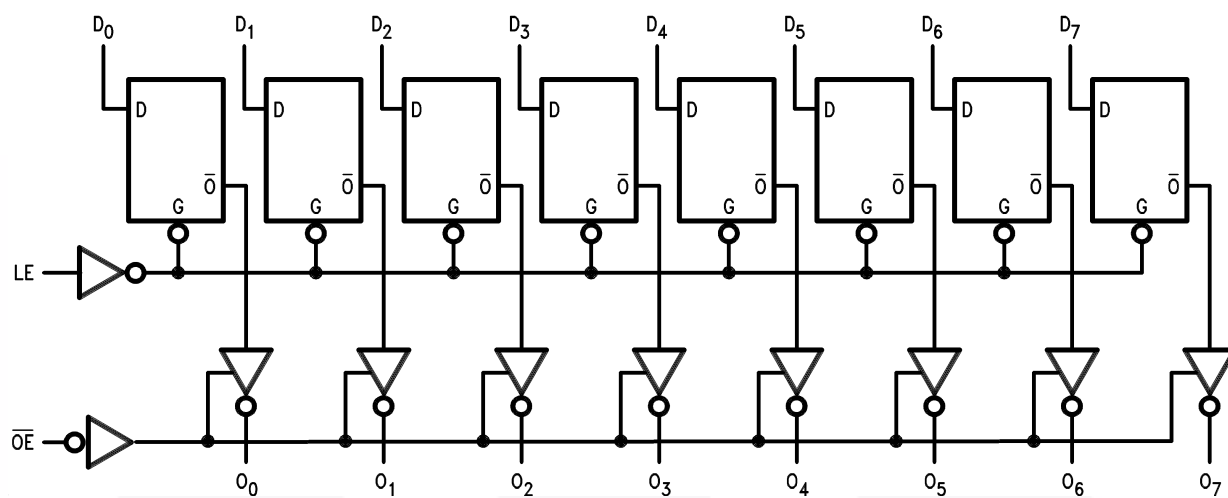
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

O₀ = Previous O₀ before HIGH-to-LOW transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------------------|--|--------------------------|
| V_{CC} | Supply Voltage | −0.5V to +7.0V |
| I_{IK} | DC Input Diode Current $V_I = -0.5V$ | −20mA |
| | $V_I = V_{CC} + 0.5$ | +20mA |
| V_I | DC Input Voltage | −0.5V to $V_{CC} + 0.5V$ |
| I_{OK} | DC Output Diode Current $V_O = -0.5V$ | −20mA |
| | $V_O = V_{CC} + 0.5V$ | +20mA |
| V_O | DC Output Voltage | −0.5V to $V_{CC} + 0.5V$ |
| I_O | DC Output Source or Sink Current | ±50mA |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current per Output Pin | ±50mA |
| T_{STG} | Storage Temperature | −65°C to +150°C |
| T_J | Junction Temperature | 140°C |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|-----------------------|--|----------------|
| V_{CC} | Supply Voltage AC | 2.0V to 6.0V |
| | ACT | 4.5V to 5.5V |
| V_I | Input Voltage | 0V to V_{CC} |
| V_O | Output Voltage | 0V to V_{CC} |
| T_A | Operating Temperature | −40°C to +85°C |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V | 125mV/ns |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V | 125mV/ns |

DC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = −40°C to +85°C | Units |
|--------------------------------|---|---------------------|--|------------------------|-------------------|---------------------------------|-------|
| | | | | Typ. | Guaranteed Limits | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} − 0.1V | 1.5 | 2.1 | 2.1 | V |
| | | 4.5 | | 2.25 | 3.15 | 3.15 | |
| | | 5.5 | | 2.75 | 3.85 | 3.85 | |
| V _{IL} | Maximum LOW Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} − 0.1V | 1.5 | 0.9 | 0.9 | V |
| | | 4.5 | | 2.25 | 1.35 | 1.35 | |
| | | 5.5 | | 2.75 | 1.65 | 1.65 | |
| V _{OH} | Minimum HIGH Level Output Voltage | 3.0 | I _{OUT} = −50μA | 2.99 | 2.9 | 2.9 | V |
| | | 4.5 | | 4.49 | 4.4 | 4.4 | |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = −12mA | | 2.56 | 2.46 | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = −24mA | | 3.86 | 3.76 | |
| | | 5.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = −24mA ⁽¹⁾ | | 4.86 | 4.76 | |
| V _{OL} | Maximum LOW Level Output Voltage | 3.0 | I _{OUT} = 50μA | 0.002 | 0.1 | 0.1 | V |
| | | 4.5 | | 0.001 | 0.1 | 0.1 | |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA | | 0.36 | 0.44 | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA | | 0.36 | 0.44 | |
| | | 5.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽¹⁾ | | 0.36 | 0.44 | |
| I _{IN} ⁽²⁾ | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ±1.0 | μA |
| I _{OZ} | Maximum 3-STATE Leakage Current | 5.5 | V _I (OE) = V _{IL} , V _{IH} ; V _I = V _{CC} , GND; V _O = V _{CC} , GND | | ±0.25 | ±2.5 | μA |
| I _{OLD} | Minimum Dynamic Output Current ⁽³⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | mA |
| I _{OHD} | | 5.5 | V _{OHD} = 3.85V Min. | | | −75 | mA |
| I _{CC} ⁽²⁾ | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 4.0 | 40.0 | μA |

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
3. Maximum test duration 2.0ms, one output loaded at a time.

DC Electrical Characteristics for ACT

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = −40°C to +85°C | | Units |
|------------------|---|---------------------|---|------------------------|-------------------|---------------------------------|--|-------|
| | | | | Typ. | Guaranteed Limits | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} − 0.1V | 1.5 | 2.0 | 2.0 | | V |
| | | 5.5 | | 1.5 | 2.0 | 2.0 | | |
| V _{IL} | Maximum LOW Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} − 0.1V | 1.5 | 0.8 | 0.8 | | V |
| | | 5.5 | | 1.5 | 0.8 | 0.8 | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 4.5 | I _{OUT} = −50μA | 4.49 | 4.4 | 4.4 | | V |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = −24mA | | 3.86 | 3.76 | | |
| | | 5.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = −24mA ⁽⁴⁾ | | 4.86 | 4.76 | | |
| V _{OL} | Maximum LOW Level Output Voltage | 4.5 | I _{OUT} = 50μA | 0.001 | 0.1 | 0.1 | | V |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA | | 0.36 | 0.44 | | |
| | | 5.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽⁴⁾ | | 0.36 | 0.44 | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ±1.0 | | μA |
| I _{OZ} | Maximum 3-STATE Leakage Current | 5.5 | V _I = V _{IL} , V _{IH} ; V _O = V _{CC} , GND | | ±0.25 | ±2.5 | | μA |
| I _{CCT} | Maximum I _{CC} /Input | 5.5 | V _I = V _{CC} − 2.1V | 0.6 | | 1.5 | | mA |
| I _{OLD} | Minimum Dynamic Output Current ⁽⁵⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA |
| I _{OHD} | | 5.5 | V _{OHD} = 3.85V Min. | | | −75 | | mA |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 4.0 | 40.0 | | μA |

Notes:

4. All outputs loaded; thresholds on input associated with output under test.
 5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC} (V)^{(6)}$ | $T_A = +25^{\circ}C$, $C_L = 50pF$ | | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $C_L = 50pF$ | | Units |
|-----------|-----------------------------------|--------------------|--|------|------|--|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| t_{PLH} | Propagation Delay, D_n to O_n | 3.3 | 1.5 | 10.0 | 13.5 | 1.5 | 15.0 | ns |
| | | 5.0 | 1.5 | 7.0 | 9.5 | 1.5 | 10.5 | |
| t_{PHL} | Propagation Delay, D_n to O_n | 3.3 | 1.5 | 9.5 | 13.0 | 1.5 | 14.5 | ns |
| | | 5.0 | 1.5 | 7.0 | 9.5 | 1.5 | 10.5 | |
| t_{PLH} | Propagation Delay, LE to O_n | 3.3 | 1.5 | 10.0 | 13.5 | 1.5 | 15.0 | ns |
| | | 5.0 | 1.5 | 7.5 | 9.5 | 1.5 | 10.5 | |
| t_{PHL} | Propagation Delay, LE to O_n | 3.3 | 1.5 | 9.5 | 12.5 | 1.5 | 14.0 | ns |
| | | 5.0 | 1.5 | 7.0 | 9.5 | 1.5 | 10.5 | |
| t_{PZH} | Output Enable Time | 3.3 | 1.5 | 9.0 | 11.5 | 1.0 | 13.0 | ns |
| | | 5.0 | 1.5 | 7.0 | 8.5 | 1.0 | 9.5 | |
| t_{PZL} | Output Enable Time | 3.3 | 1.5 | 8.5 | 11.5 | 1.0 | 13.0 | ns |
| | | 5.0 | 1.5 | 6.5 | 8.5 | 1.0 | 9.5 | |
| t_{PHZ} | Output Disable Time | 3.3 | 1.5 | 10.0 | 12.5 | 1.0 | 14.5 | ns |
| | | 5.0 | 1.5 | 8.0 | 11.0 | 1.0 | 12.5 | |
| t_{PLZ} | Output Disable Time | 3.3 | 1.5 | 8.0 | 11.5 | 1.0 | 12.5 | ns |
| | | 5.0 | 1.5 | 6.5 | 8.5 | 1.0 | 10.0 | |

Note:

6. Voltage range 3.3 is $3.3V \pm 0.3V$. Voltage range 5.0 is $5.0V \pm 0.5V$.

AC Operating Requirements for AC

| Symbol | Parameter | V _{CC} (V) ⁽⁷⁾ | T _A = +25°C, C _L = 50pF | | T _A = −40°C to +85°C, C _L = 50pF | Units |
|----------------|---|------------------------------------|--|--------------------|---|-------|
| | | | Typ | Guaranteed Minimum | | |
| t _S | Setup Time, HIGH or LOW, D _n to LE | 3.3 | 3.5 | 5.5 | 6.0 | ns |
| | | 5.0 | 2.0 | 4.0 | 4.5 | |
| t _H | Hold Time, HIGH or LOW, D _n to LE | 3.3 | −3.0 | 1.0 | 1.0 | ns |
| | | 5.0 | −1.5 | 1.0 | 1.0 | |
| t _W | LE Pulse Width, HIGH | 3.3 | 4.0 | 5.5 | 6.0 | ns |
| | | 5.0 | 2.0 | 4.0 | 4.5 | |

Note:

7. Voltage range 3.3 is $3.3V \pm 0.3V$. Voltage range 5.0 is $5.0V \pm 0.5V$.

AC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC} (V)^{(8)}$ | $T_A = +25^{\circ}C,$ $C_L = 50pF$ | | | $T_A = -40^{\circ}C \text{ to } +85^{\circ}C,$ $C_L = 50pF$ | | Units |
|-----------|-----------------------------------|--------------------|---------------------------------------|------|------|--|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| t_{PLH} | Propagation Delay, D_n to O_n | 5.0 | 2.5 | 8.5 | 10.0 | 1.5 | 11.5 | ns |
| t_{PHL} | Propagation Delay, D_n to O_n | 5.0 | 2.0 | 8.0 | 10.0 | 1.5 | 11.5 | ns |
| t_{PLH} | Propagation Delay, LE to O_n | 5.0 | 2.5 | 8.5 | 11.0 | 2.0 | 11.5 | ns |
| t_{PHL} | Propagation Delay, LE to O_n | 5.0 | 2.0 | 8.0 | 10.0 | 1.5 | 11.5 | ns |
| t_{PZH} | Output Enable Time | 5.0 | 2.0 | 8.0 | 9.5 | 1.5 | 10.5 | ns |
| t_{PZL} | Output Enable Time | 5.0 | 2.0 | 7.5 | 9.0 | 1.5 | 10.5 | ns |
| t_{PHZ} | Output Disable Time | 5.0 | 2.5 | 9.0 | 11.0 | 2.5 | 12.5 | ns |
| t_{PLZ} | Output Disable Time | 5.0 | 1.5 | 7.5 | 8.5 | 1.0 | 10.0 | ns |

Note:

8. Voltage range 5.0 is $5.0V \pm 0.5V$.

AC Operating Requirements for ACT

| Symbol | Parameter | V _{CC} (V) ⁽⁹⁾ | T _A = +25°C, C _L = 50pF | | T _A = −40°C to +85°C, C _L = 50pF | Units |
|----------------|--|------------------------------------|--|--------------------|---|-------|
| | | | Typ | Guaranteed Minimum | | |
| t _S | Setup Time, HIGH or LOW, D _n to LE | 5.0 | 0.8 | 2.5 | 3.5 | ns |
| t _H | Hold Time, HIGH or LOW, D _n to LE | 5.0 | 0 | 0 | 1.0 | ns |
| t _W | LE Pulse Width, HIGH | 5.0 | 2.0 | 7.0 | 8.0 | ns |

Note:

9. Voltage range 5.0 is $5.0V \pm 0.5V$.

Capacitance

| Symbol | Parameter | Conditions | Typ. | Units |
|----------|-------------------------------|------------------------|------|-------|
| C_{IN} | Input Capacitance | $V_{CC} = \text{OPEN}$ | 4.5 | pF |
| C_{PD} | Power Dissipation Capacitance | $V_{CC} = 5.0V$ | 40.0 | pF |

Physical Dimensions

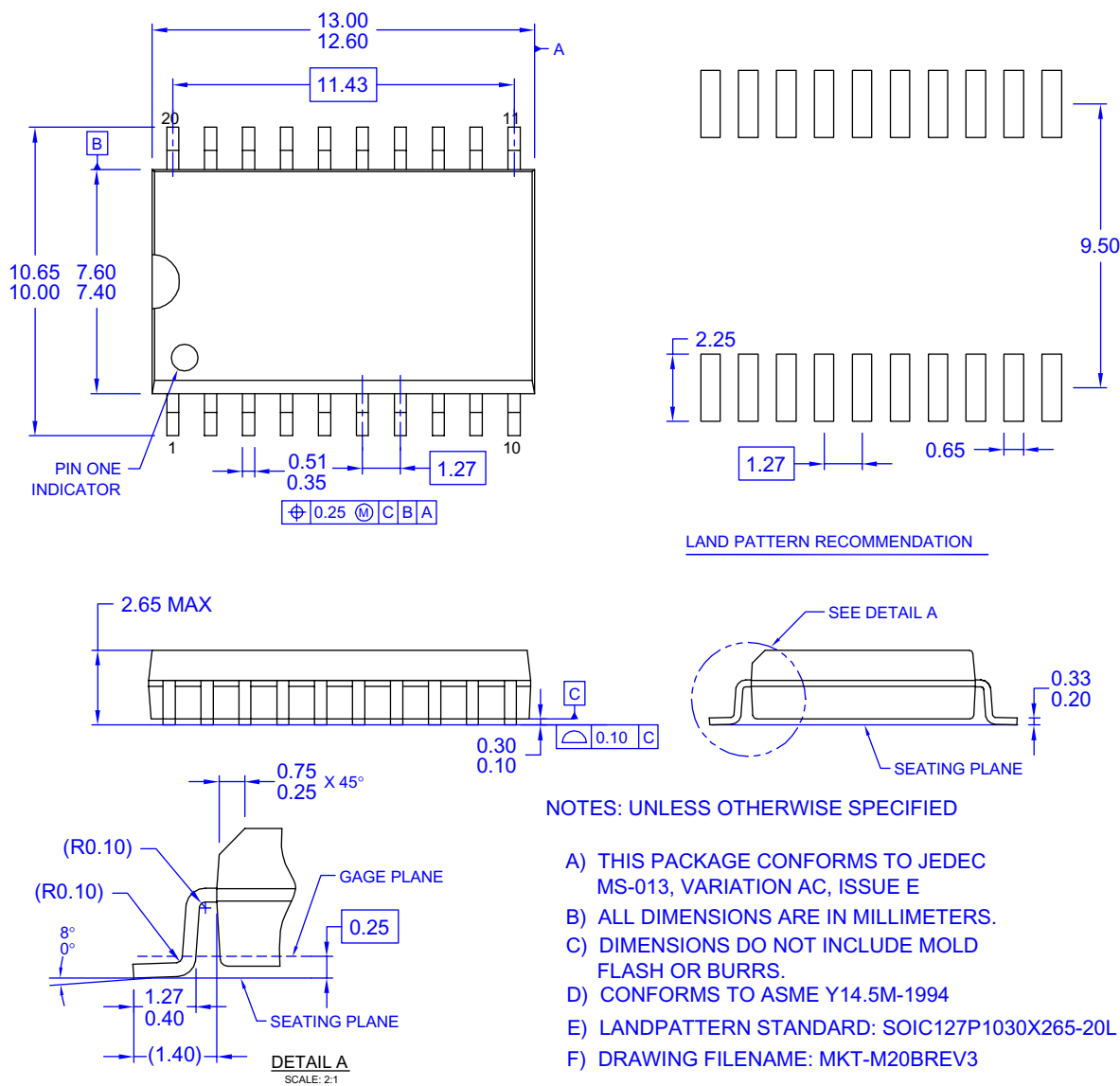


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)

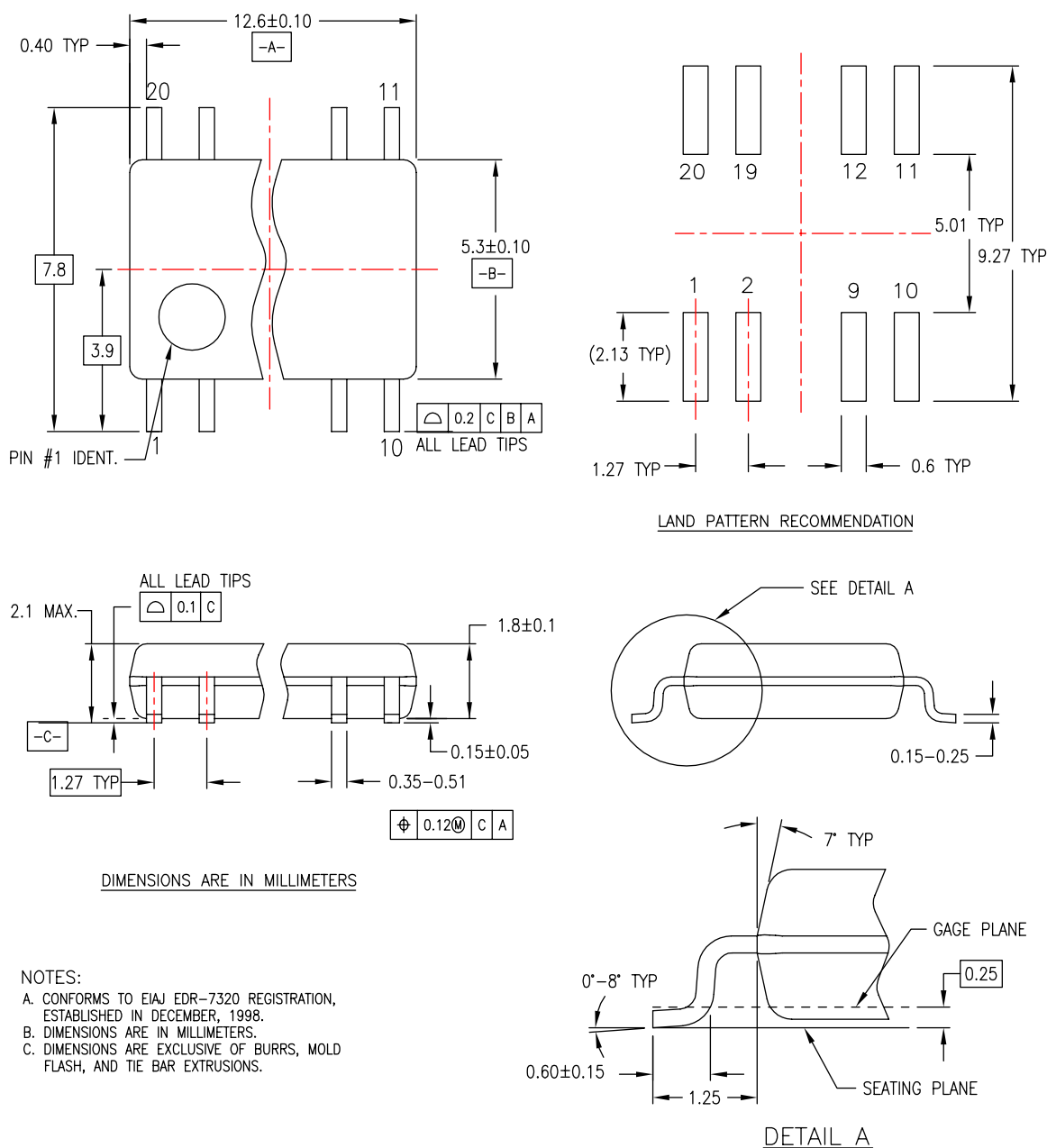


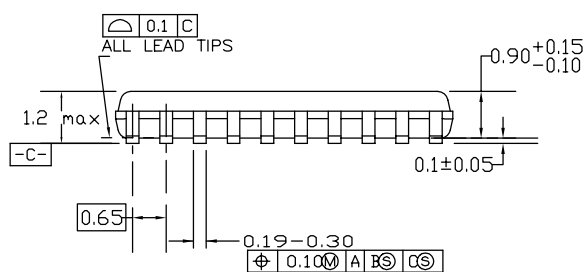
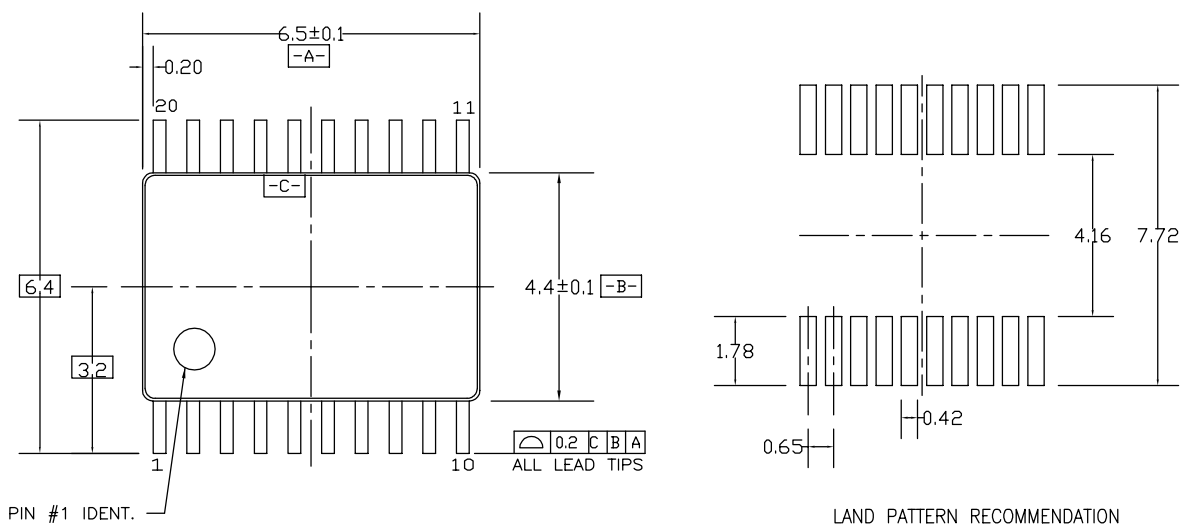
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

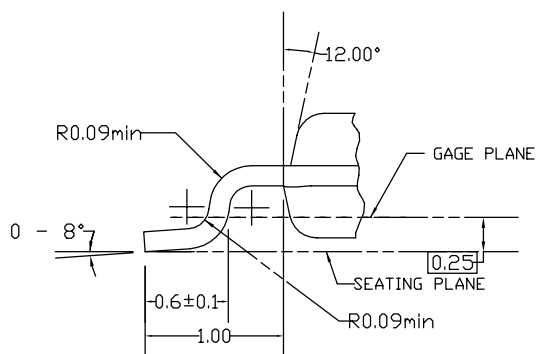
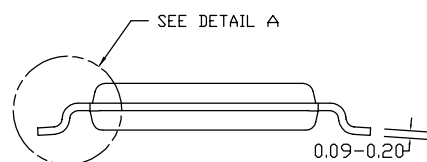
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

- CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

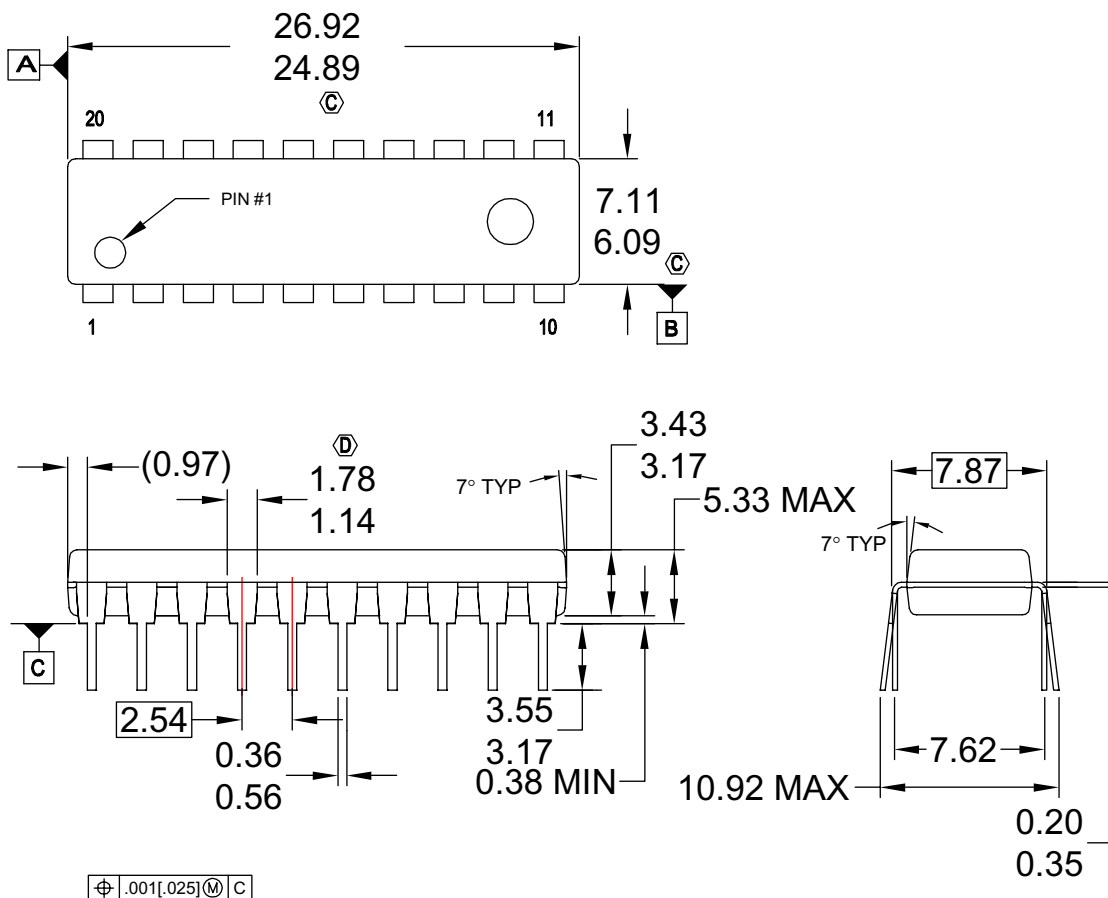
Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- F. DRAWING FILE NAME: N20AREV8

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.



Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

| | | | |
|---|--|--|----------------------------------|
| ACEx [®] | FPS [™] | PDP-SPM [™] | SyncFET [™] |
| Build it Now [™] | FRFET [®] | Power220 [®] | SYSTEM [®] |
| CorePLUS [™] | Global Power Resource SM | Power247 [®] | GENERAL |
| CROSSVOLT [™] | Green FPS [™] | POWEREDGE [®] | The Power Franchise [®] |
| CTL [™] | Green FPS [™] e-Series [™] | Power-SPM [™] | the power [™] |
| Current Transfer Logic [™] | GTO [™] | PowerTrench [®] | franchise |
| EcoSPARK [®] | i-Lo [™] | Programmable Active Droop [™] | TinyBoost [™] |
| EZSWITCH [™] * | IntelliMAX [™] | QFET [®] | TinyBuck [™] |
|  | ISOPLANAR [™] | QS [™] | TinyLogic [®] |
|  | MegaBuck [™] | QT Optoelectronics [™] | TINYOPTO [™] |
| Fairchild [®] | MICROCOUPLER [™] | Quiet Series [™] | TinyPower [™] |
| Fairchild Semiconductor [®] | MicroFET [™] | RapidConfigure [™] | TinyPWM [™] |
| FACT Quiet Series [™] | MicroPak [™] | SMART START [™] | TinyWire [™] |
| FACT [®] | MillerDrive [™] | SPM [®] | μSerDes [™] |
| FAST [®] | Motion-SPM [™] | STEALTH [™] | UHC [®] |
| FastvCore [™] | OPTOLOGIC [®] | SuperFET [™] | Ultra FRFET [™] |
| FlashWriter [®] * | OPTOPLANAR [®] | SuperSOT [™] -3 | UniFET [™] |
| | | SuperSOT [™] -6 | VCX [™] |
| | | SuperSOT [™] -8 | |

* EZSWITCH[™] and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

| Datasheet Identification | Product Status | Definition |
|--------------------------|------------------------|--|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only. |

Rev. I32

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Fairchild Semiconductor:

[74ACT373MSA](#) [74ACT373MTC](#) [74ACT373MTCX](#) [74ACT373SCX](#) [74ACT373SC](#) [74ACT373SJ](#) [74ACT373PC](#)
[74ACT373MSAX](#) [74ACT373SJX](#)