National Semiconductor

June 2007

LMP7707/LMP7708/LMP7709 Precision, CMOS Input, RRIO, Wide Supply Range Decompensated Amplifiers

General Description

The LMP7707/LMP7708/LMP7709 devices are single, dual, and quad low offset voltage, rail-to-rail input and output precision amplifiers which each have a CMOS input stage and a wide supply voltage range. The LMP7707/LMP7708/LMP7709 are part of the LMP® precision amplifier family and are ideal for sensor interface and other instrumentation applications. These decompensated amplifiers are stable at a gain of 6 and higher.

The guaranteed low offset voltage of less than ±200 μV along with the guaranteed low input bias current of less than ±1 pA make the LMP7707/LMP7708/LMP7709 ideal for precision applications. The LMP7707/LMP7708/LMP7709 are built utilizing VIP50 technology, which allows the combination of a CMOS input stage and a supply voltage range of 12V with rail-to-rail common mode voltage capability. The LMP7707/LMP7708/LMP7709 are the perfect choice in many applications where conventional CMOS parts cannot operate due to the voltage conditions.

The unique design of the rail-to-rail input stage of each of the LMP7707/LMP7708/LMP7709 significantly reduces the CMRR glitch commonly associated with rail-to-rail input amplifiers. Both sides of the complimentary input stage have been trimmed, thereby reducing the difference between the NMOS and PMOS offsets. The output swings within 40 mV of either rail to maximize the signal dynamic range in applications requiring low supply voltage.

The LMP7707 is offered in the space saving 5-Pin SOT23 package, the LMP7708 is offered in the 8-Pin MSOP and the quad LMP7709 is offered in the 14-Pin TSSOP package. These small packages are ideal solutions for area constrained PC boards and portable electronics.

Features

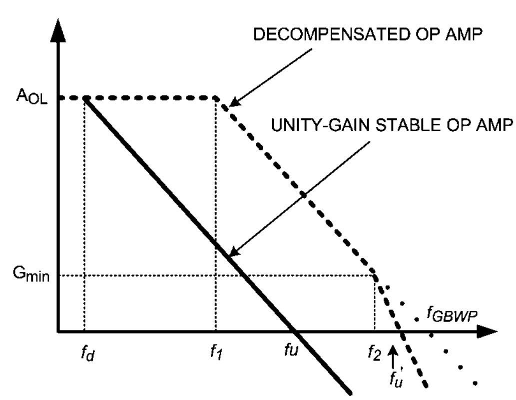
Unless otherwise noted, typical values at $V_S = 5V$.

- Input offset voltage (LMP7707) ±200 μV (max)
- Input offset voltage (LMP7708/LMP7709) ±220 μV (max)
- Input bias current ±200 fA
- Input voltage noise 9 nV/√Hz
- CMRR 130 dB
- Open loop gain 130 dB
- Temperature range −40°C to 125°C
- Gain bandwidth product (A_V =10) 14 MHz
- Stable at a gain of 10 or higher
- Supply current (LMP7707) 715 μA
- Supply current (LMP7708) 1.5 mA
- Supply current (LMP7709) 2.9 mA
- Supply voltage range 2.7V to 12V
- Rail-to-rail input and output

Applications

- High impedance sensor interface
- Battery powered instrumentation
- High gain amplifiers
- DAC buffer
- Instrumentation amplifier
- Active filters

Open Loop Frequency Response



Increased Bandwidth for Same Supply Current at A_V> 10

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	200V
Charge Device Model	1000V
V_{IN} Differential	±300 mV
Supply Voltage ($V_S = V^+ – V^–$)	13.2V
Voltage at Input/Output Pins	V^++ 0.3V to V^- – 0.3V
Input Current	10 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

Operating Ratings (Note 1)

Temperature Range (Note 3)	−40°C to +125°C
Supply Voltage ($V_S = V^+ – V^–$)	2.7V to 12V
Package Thermal Resistance (θ_{JA}) (Note 3)	
5-Pin SOT23	265°C/W
8-Pin MSOP	235°C/W
14-Pin TSSOP	122°C/W

3V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 3V, V^- = 0V, $V_{CM} = V^+/2$, and R_L > 10 kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	LMP7707		±37	±200 **±500**	μV
		LMP7708/LMP7709		±56	±220 **±520**	
TCV_{OS}	Input Offset Voltage Drift (Note 7)			±1	**±5**	μV/°C
I_B	Input Bias Current (Notes 7, 8)			±0.2	±1	pA
		−40°C ≤ T_A ≤ 85°C			±50	
		−40°C ≤ T_A ≤ 125°C			±400	
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V LMP7707	86 **80**	130		dB
		0V ≤ V_{CM} ≤ 3V LMP7708/LMP7709	84 **78**	130		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, Vo = $V^+/2$	86 **82**	98		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB	−0.2		3.2	V
		CMRR ≥ 77 dB	**−0.2**		**3.2**	
A_{VOL}	Open Loop Voltage Gain	R_L = 2 kΩ (LMP7707) V_O = 0.3V to 2.7V	100 **96**	114		dB
		R_L = 2 kΩ (LMP7708/LMP7709) V_O = 0.3V to 2.7V	100 **94**	114		
		R_L = 10 kΩ V_O = 0.2V to 2.8V	100 **96**	124		

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$ LMP7707		40	80 **120**	mV from V^+
		R_L = 2 kΩ to $V^+/2$ LMP7708/LMP7709		40	80 **150**	
		R_L = 10 kΩ to $V^+/2$ LMP7707		30	40 **60**	
		R_L = 10 kΩ to $V^+/2$ LMP7708/LMP7709		35	50 **100**	
	Output Swing Low	R_L = 2 kΩ to $V^+/2$ LMP7707		40	60 **80**	mV
		R_L = 2 kΩ to $V^+/2$ LMP7708/LMP7709		45	100 **170**	
		R_L = 10 kΩ to $V^+/2$ LMP7707		20	40 **50**	
		R_L = 10 kΩ to $V^+/2$ LMP7708/LMP7709		20	50 **90**	
I_O	Output Short Circuit Current (Notes 3, 9)	Sourcing $V_O = V^+/2$ V_{IN} = 100 mV	25 **15**	42		mA
		Sinking $V_O = V^+/2$ V_{IN} = −100 mV (LMP7707)	25 **20**	42		
		Sinking $V_O = V^+/2$ V_{IN} = −100 mV (LMP7708/ LMP7709)	25 **15**	42		
I_S	Supply Current	LMP7707		0.670	1.0 **1.2**	mA
		LMP7708		1.4	1.8 **2.1**	
		LMP7709		2.9	3.5 **4.5**	
SR	Slew Rate (Note 10)	V_O = 2 V_{PP}, 10% to 90%		5.1		V/µs
GBWP	Gain Bandwidth Product	A_V = 10		13		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 10, V_O = 2.5V, R_L = 10 kΩ		0.024		%
e_n	Input-Referred Voltage Noise	f = 1 kHz		9		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 100 kHz		1		$fA/\sqrt{Hz}$

5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V^+/2$, and R_L > 10 kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	LMP7707		±37	±200 **±500**	µV
		LMP7708/LMP7709		±32	±220 **±520**	
TCV_{OS}	Input Offset Voltage Drift (Note 7)			±1	**±5**	µV/°C
I_B	Input Bias Current (Notes 7, 8)			±0.2	±1	pA
		−40°C ≤ T_A ≤ 85°C			±50	
		−40°C ≤ T_A ≤ 125°C			±400	

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 5V$ LMP7707	88 **83**	130		dB
		$0V \le V_{CM} \le 5V$ LMP7708/LMP7709	86 **81**	130		
PSRR	Power Supply Rejection Ratio	$2.7V \le V^+ \le 12V$, $V_O = V^+/2$	86 **82**	100		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB	−0.2		5.2	V
		CMRR ≥ 78 dB	**−0.2**		**5.2**	
A_{VOL}	Open Loop Voltage Gain	$R_L = 2\ k\Omega$ (LMP7707) $V_O = 0.3V$ to 4.7V	100 **96**	119		dB
		$R_L = 2\ k\Omega$ (LMP7708/LMP7709) $V_O = 0.3V$ to 4.7V	100 **94**	119		
		$R_L = 10\ k\Omega$ $V_O = 0.2V$ to 4.8V	100 **96**	130		
V_O	Output Swing High	$R_L = 2\ k\Omega$ to $V^+/2$ LMP7707		60	110 **130**	mV from V+
		$R_L = 2\ k\Omega$ to $V^+/2$ LMP7708/LMP7709		60	120 **200**	
		$R_L = 10\ k\Omega$ to $V^+/2$ LMP7707		40	50 **70**	
		$R_L = 10\ k\Omega$ to $V^+/2$ LMP7708/LMP7709		40	60 **120**	
	Output Swing Low	$R_L = 2\ k\Omega$ to $V^+/2$ LMP7707		50	80 **90**	mV
		$R_L = 2\ k\Omega$ to $V^+/2$ LMP7708/LMP7709		50	120 **190**	
		$R_L = 10\ k\Omega$ to $V^+/2$ LMP7707		30	40 **50**	
		$R_L = 10\ k\Omega$ to $V^+/2$ LMP7708/LMP7709		30	50 **100**	
I_O	Output Short Circuit Current (Notes 3, 9)	Sourcing $V_O = V^+/2$ $V_{IN} = 100\ mV$ (LMP7707)	40 **28**	66		mA
		Sourcing $V_O = V^+/2$ $V_{IN} = 100\ mV$ (LMP7708/LMP7709)	38 **25**	66		
		Sinking $V_O = V^+/2$ $V_{IN} = -100\ mV$ (LMP7707)	40 **28**	76		
		Sinking $V_O = V^+/2$ $V_{IN} = -100\ mV$ (LMP7708/ LMP7709)	40 **23**	76		
I_S	Supply Current	LMP7707		0.715	1.0 **1.2**	mA
		LMP7708		1.5	1.9 **2.2**	
		LMP7709		2.9	3.7 **4.6**	
SR	Slew Rate (Note 10)	$V_O = 4\ V_{PP}$, 10% to 90%		5.6		V/μs
GBWP	Gain Bandwidth Product	$A_V = 10$		14		MHz

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 10, V_O = 4.5V, R_L = 10 kΩ		0.024		%
e_n	Input-Referred Voltage Noise	f = 1 kHz		9		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 100 kHz		1		$fA/\sqrt{Hz}$

±5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 5V, V^- = –5V, V_{CM} = 0V, and R_L > 10 kΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	LMP7707		±37	±200 **±500**	μV
		LMP7708/LMP7709		±37	±220 **±520**	
TCV_{OS}	Input Offset Voltage Drift (Note 7)			±1	**±5**	μV/°C
I_B	Input Bias Current (Notes 7, 8)			±0.2	1	pA
		−40°C ≤ T_A ≤ 85°C			±50	
		−40°C ≤ T_A ≤ 125°C			±400	
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	−5V ≤ V_{CM} ≤ 5V LMP7707	92 **88**	138		dB
		−5V ≤ V_{CM} ≤ 5V LMP7708/LMP7709	90 **86**	138		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, V^- = 0V, V_O = V^+/2	86 **82**	98		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB	−5.2		5.2	V
		CMRR ≥ 78 dB	**−5.2**		**5.2**	
A_{VOL}	Open Loop Voltage Gain	R_L = 2 kΩ (LMP7707) V_O = −4.7V to 4.7V	100 **98**	121		dB
		R_L = 2 kΩ (LMP7708/LMP7709) V_O = −4.7V to 4.7V	100 **94**	121		
		R_L = 10 kΩ (LMP7707) V_O = −4.8V to 4.8V	100 **98**	134		
		R_L = 10 kΩ (LMP7708/LMP7709) V_O = −4.8V to 4.8V	100 **97**	134		

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_O	Output Swing High	R_L = 2 kΩ to 0V LMP7707		90	150 **170**	mV from V+
		R_L = 2 kΩ to 0V LMP7708/LMP7709		90	180 **290**	
		R_L = 10 kΩ to 0V LMP7707		40	80 **100**	
		R_L = 10 kΩ to 0V LMP7708/LMP7709		40	80 **150**	
	Output Swing Low	R_L = 2 kΩ to 0V LMP7707		90	130 **150**	mV from V−
		R_L = 2 kΩ to 0V LMP7708/LMP7709		90	180 **290**	
		R_L = 10 kΩ to 0V LMP7707		40	50 **60**	
		R_L = 10 kΩ to 0V LMP7708/LMP7709		40	60 **110**	
I_O	Output Short Circuit Current (Notes 3, 9)	Sourcing V_O = 0V V_{IN} = 100 mV (LMP7707)	50 **35**	86		mA
		Sourcing V_O = 0V V_{IN} = 100 mV (LMP7708/LMP7709)	48 **33**	86		
		Sinking V_O = 0V V_{IN} = −100 mV	50 **35**	84		
I_S	Supply Current	LMP7707		0.790	1.1 **1.3**	mA
		LMP7708		1.7	2.1 **2.5**	
		LMP7709		3.2	4.2 **5.0**	
SR	Slew Rate (Note 10)	V_O = 9 V_{PP}, 10% to 90%		5.9		V/μs
GBWP	Gain Bandwidth Product	A_V = 10		15		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 10, V_O = 9V, R_L = 10 kΩ		0.024		%
e_n	Input-Referred Voltage Noise	f = 1 kHz		9		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 100 kHz		1		$fA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)
Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

Note 7: This parameter is guaranteed by design and/or characterization and is not tested in production.

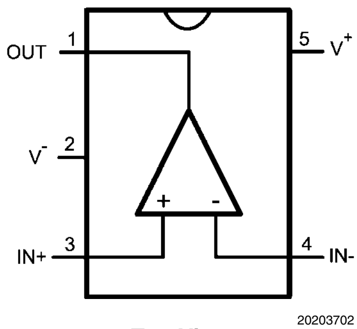
Note 8: Positive current corresponds to current flowing into the device.

Note 9: The short circuit test is a momentary test.

Note 10: The number specified is the slower of positive and negative slew rates.

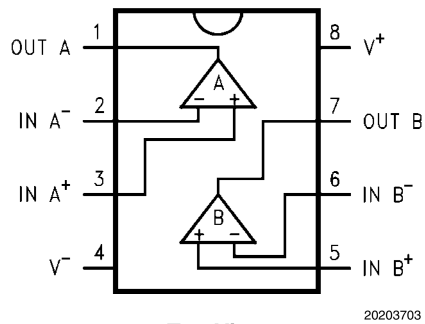
Connection Diagrams

5-Pin SOT23



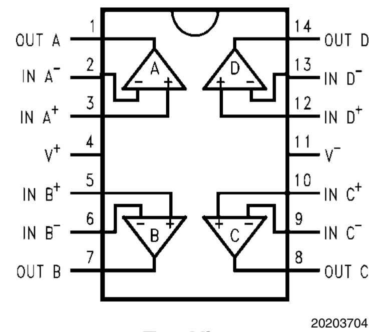
Top View

8-Pin MSOP



Top View

14-Pin TSSOP



Top View

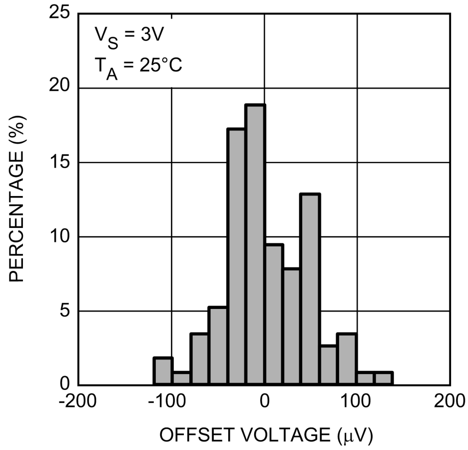
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT23	LMP7707MF	AH4A	1k Units Tape and Reel	MF05A
	LMP7707MFX		3k Units Tape and Reel	
8-Pin MSOP	LMP7708MM	AJ4A	1k Units Tape and Reel	MUA08A
	LMP7708MMX		3.5k Units Tape and Reel	
14-Pin TSSOP	LMP7709MT	LMP7709MT	94 Units/Rail	MTC14
	LMP7709MTX		2.5k Units Tape and Reel	

Typical Performance Characteristics

Unless otherwise specified, $T_A = 25°C$, $V_{CM} = V_S/2$, $R_L > 10\ k\Omega$ connected to $(V^+ + V^-)/2$

Offset Voltage Distribution



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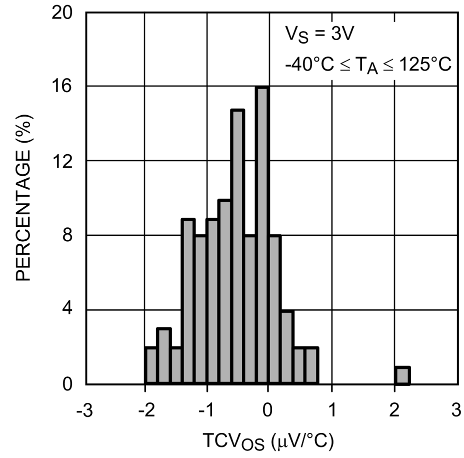
TCVOS Distribution



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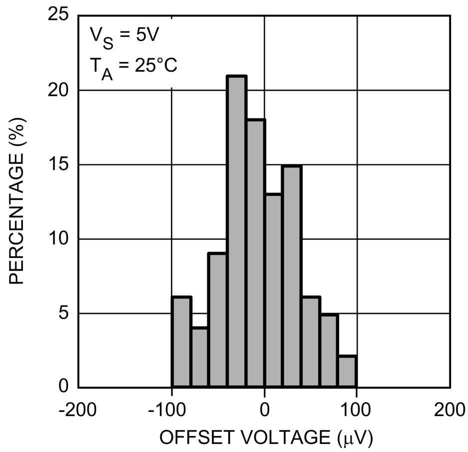
Offset Voltage Distribution



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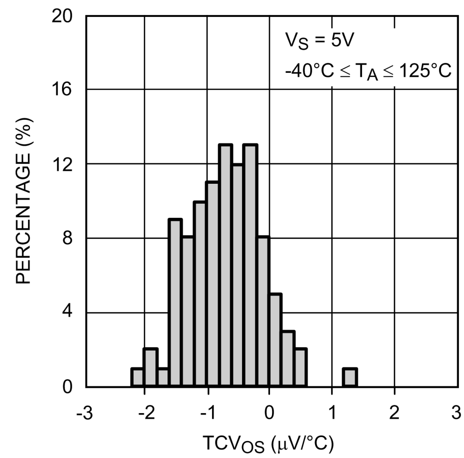

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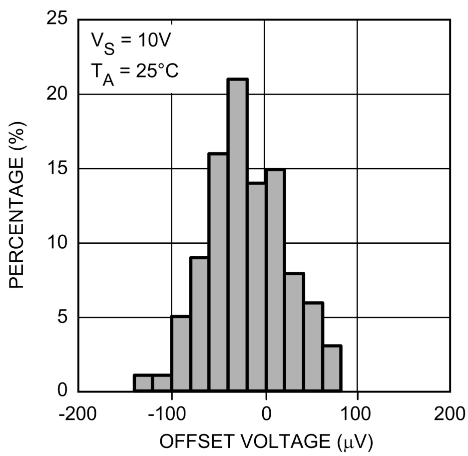
Offset Voltage Distribution



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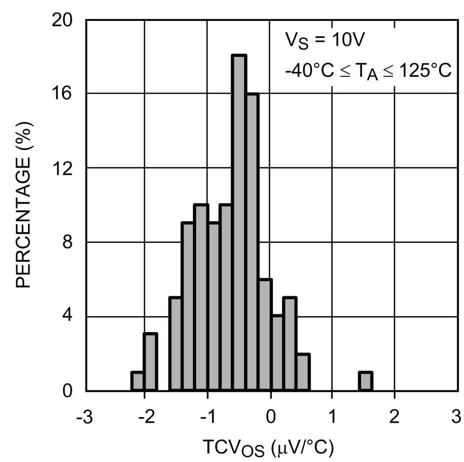
TCVOS Distribution



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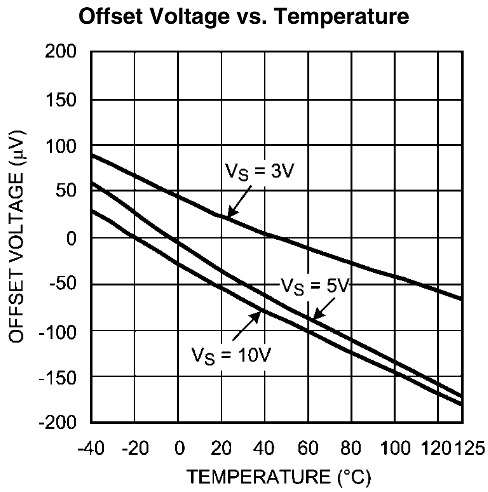

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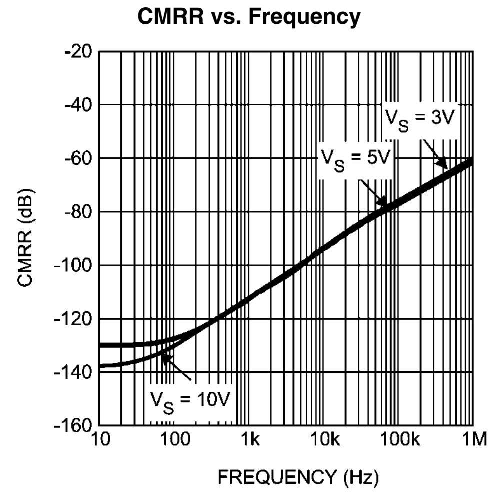

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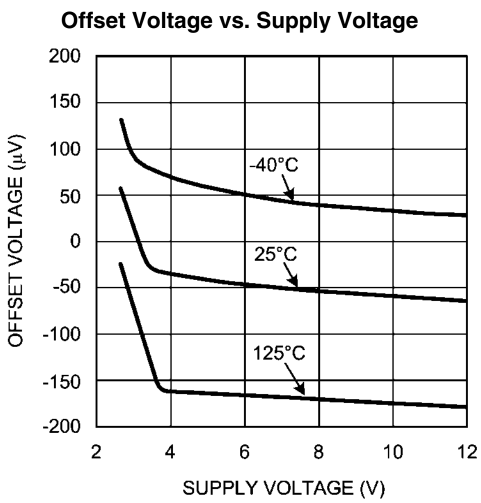

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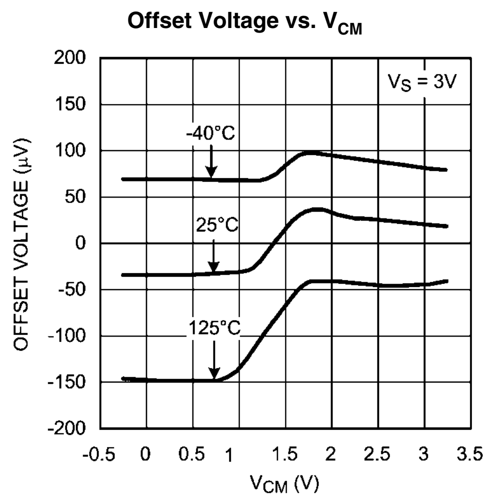

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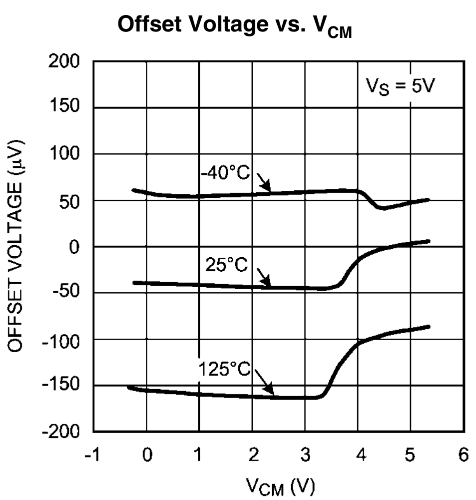

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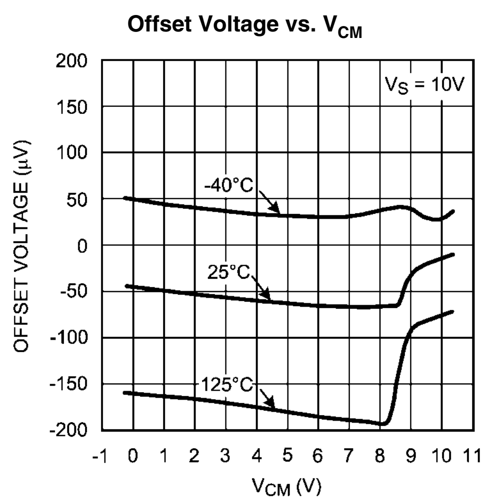

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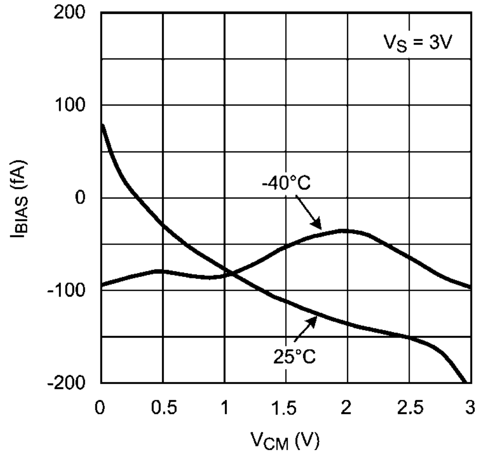
Input Bias Current vs. V_{CM}



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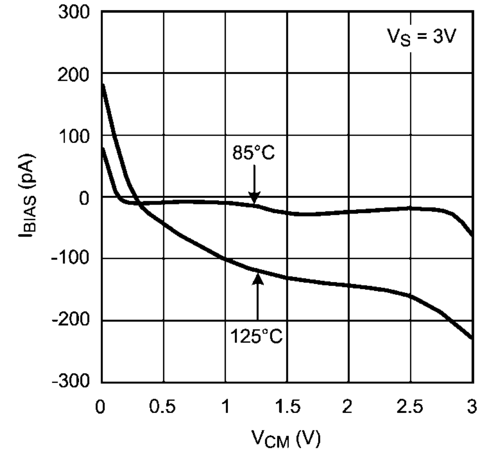
Input Bias Current vs. V_{CM}



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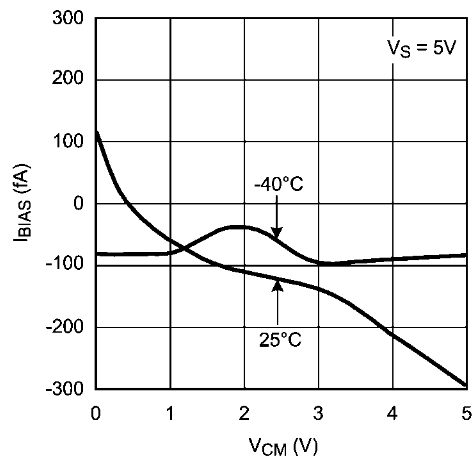
Input Bias Current vs. V_{CM}



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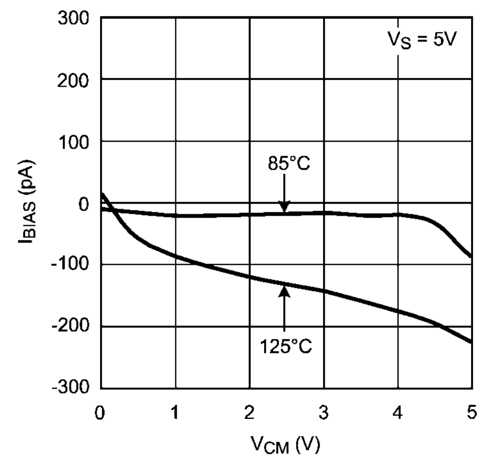
Input Bias Current vs. V_{CM}



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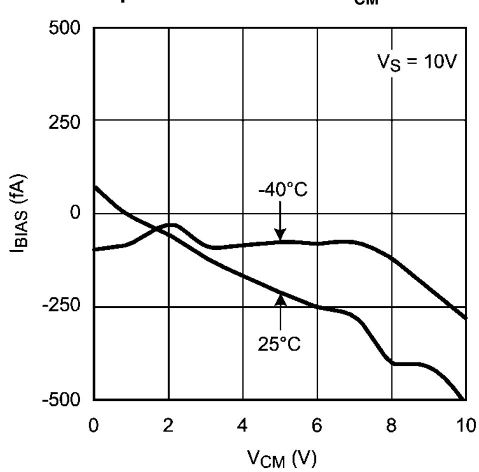
Input Bias Current vs. V_{CM}



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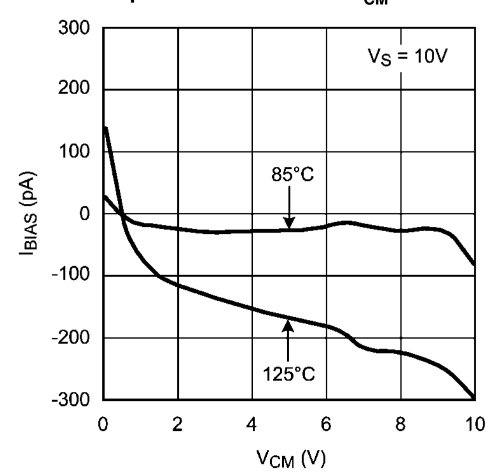
Input Bias Current vs. V_{CM}



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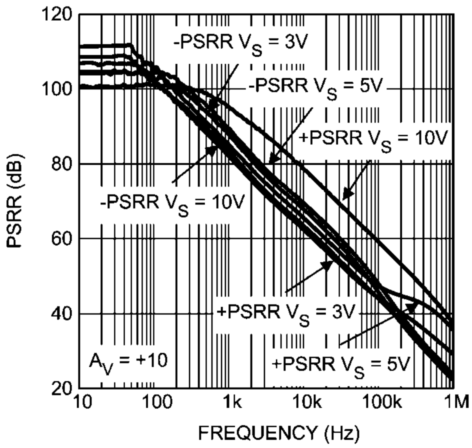
PSRR vs. Frequency



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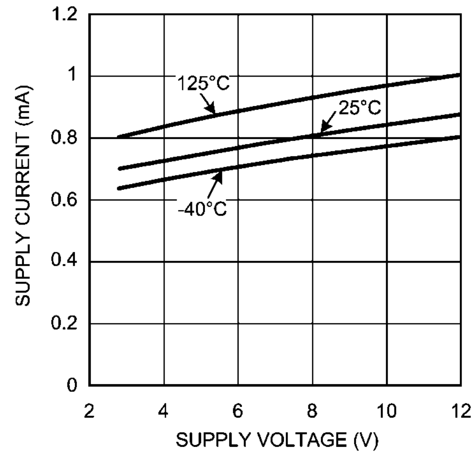
Supply Current vs. Supply Voltage (Per Channel)



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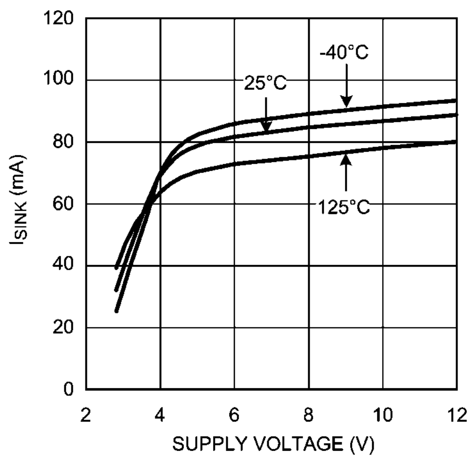
Sinking Current vs. Supply Voltage



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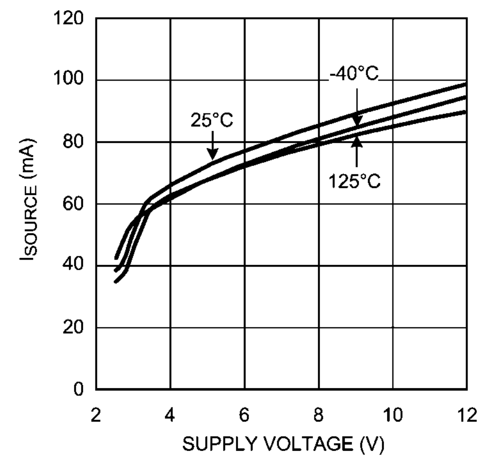
Sourcing Current vs. Supply Voltage



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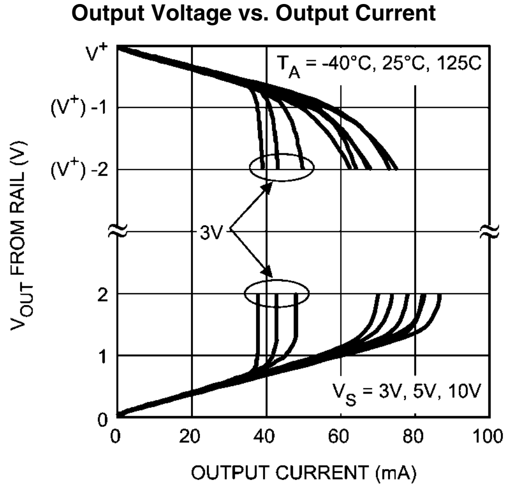
Output Voltage vs. Output Current



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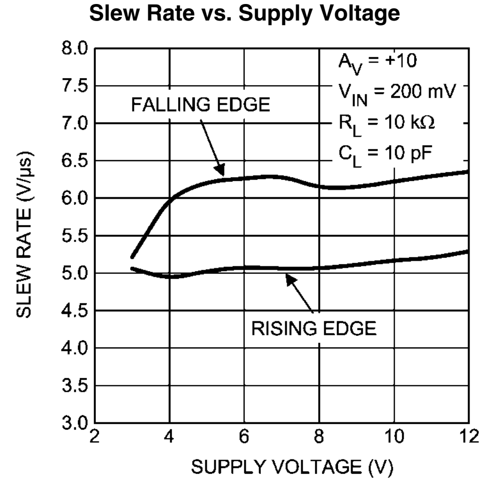
Slew Rate vs. Supply Voltage



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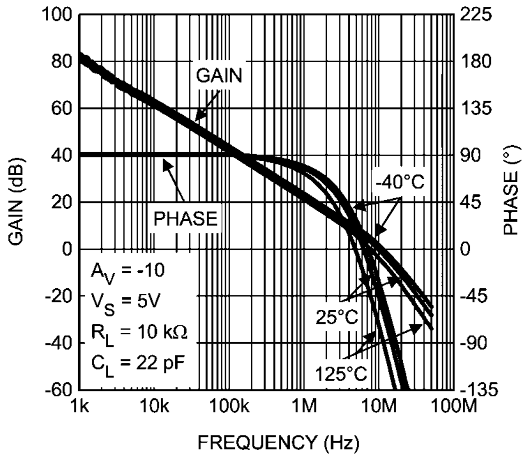
Open Loop Frequency Response



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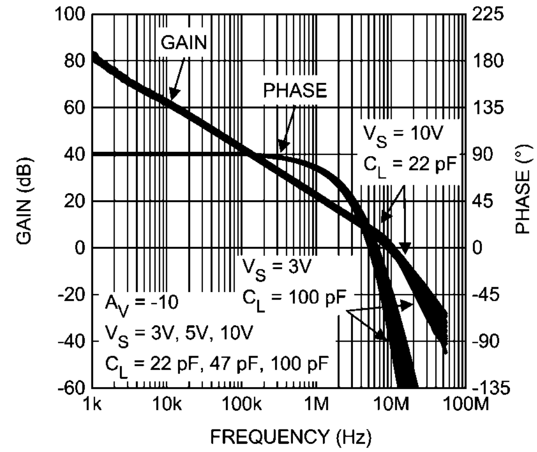
Open Loop Frequency Response



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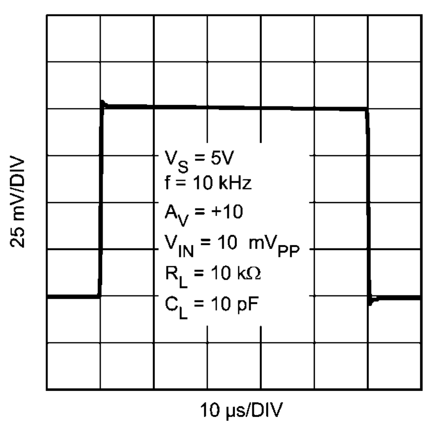
Small Signal Step Response, A_V = 10



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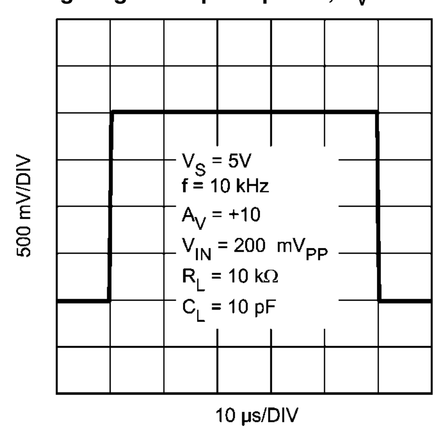
Large Signal Step Response, A_V = 10



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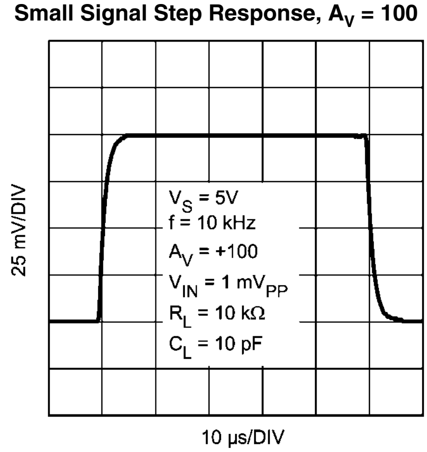
Small Signal Step Response, A_V = 100



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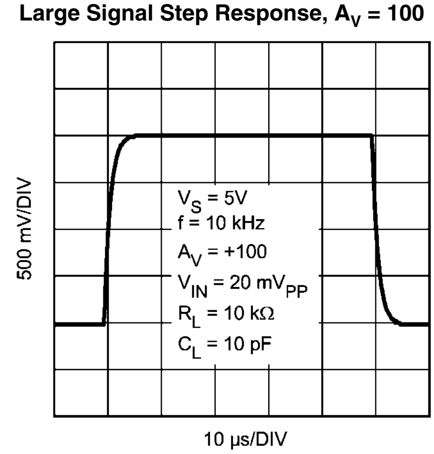
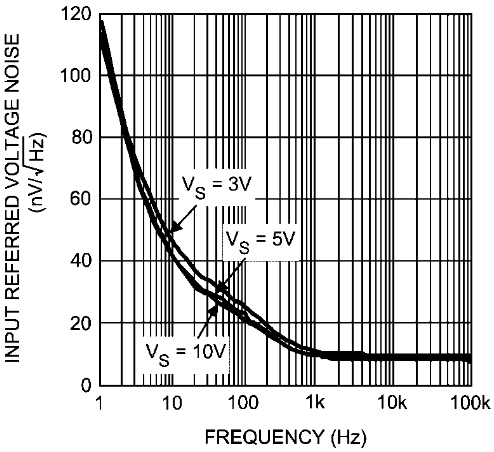
Large Signal Step Response, A_V = 100



20203720

Input Voltage Noise vs. Frequency



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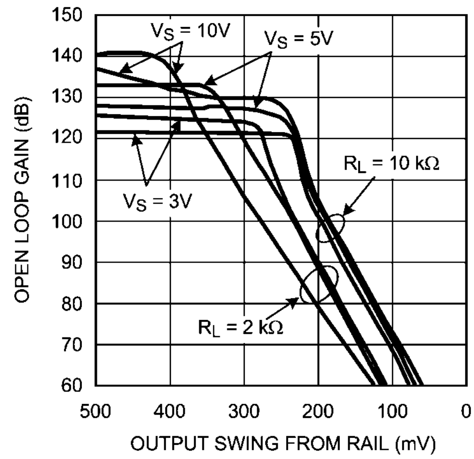
Open Loop Gain vs. Output Voltage Swing



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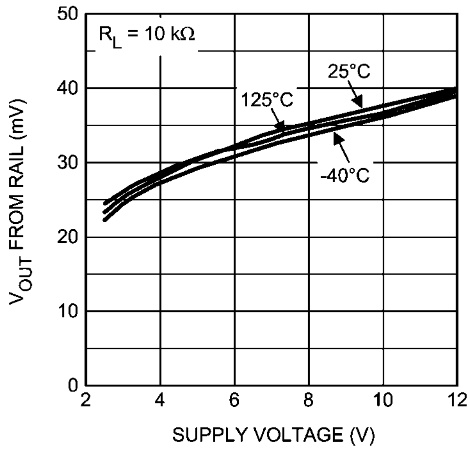
Output Swing High vs. Supply Voltage



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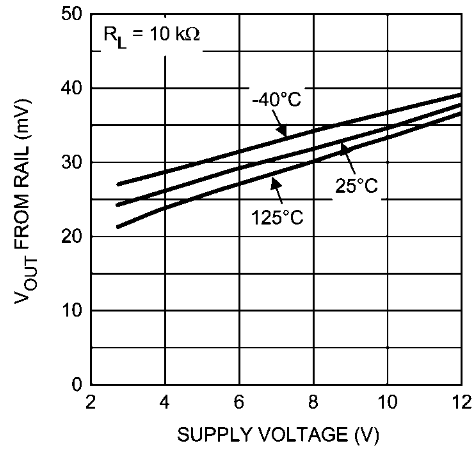
Output Swing Low vs. Supply Voltage



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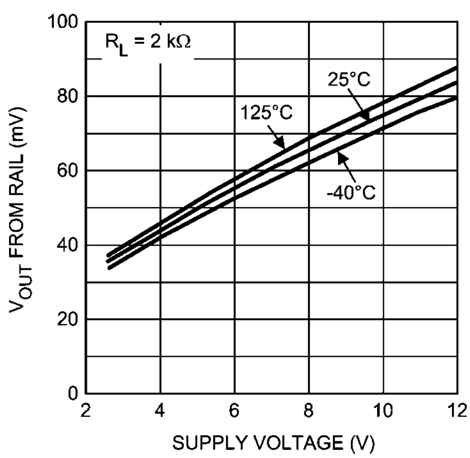
Output Swing High vs. Supply Voltage



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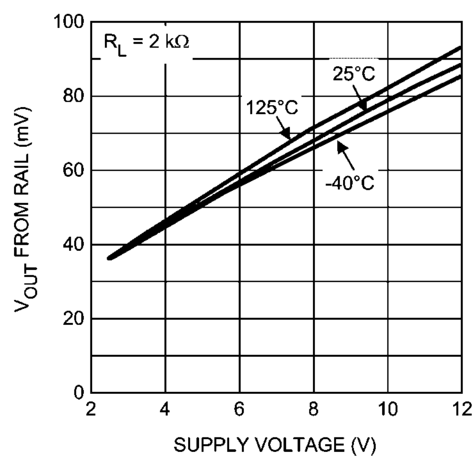
Output Swing Low vs. Supply Voltage



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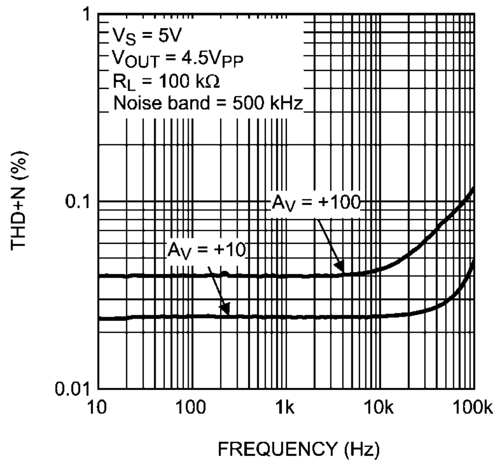
THD+N vs. Frequency



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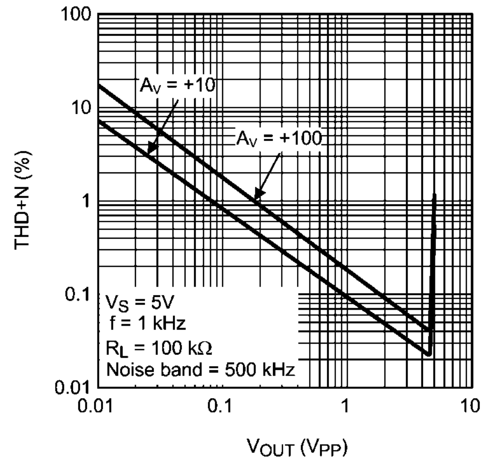
THD+N vs. Output Voltage



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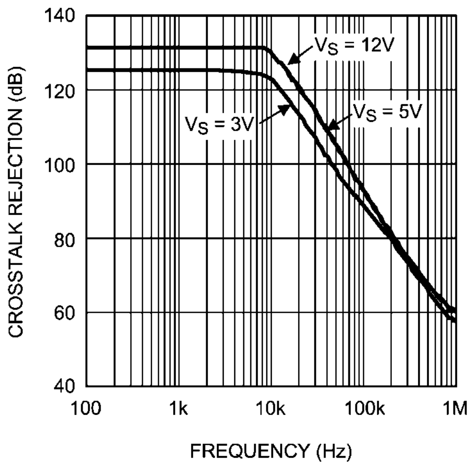
Crosstalk Rejection Ratio vs. Frequency (LMP7708/LMP7709)



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Application Information

LMP7707/LMP7708/LMP7709

The LMP7707/LMP7708/LMP7709 devices are single, dual and quad low offset voltage, rail-to-rail input and output precision amplifiers each with a CMOS input stage and the wide supply voltage range of 2.7V to 12V. The LMP7707/LMP7708/LMP7709 have a very low input bias current of only ±200 fA at room temperature.

The wide supply voltage range of 2.7V to 12V over the extensive temperature range of −40°C to 125°C makes either the LMP7707, LMP7708 or LMP7709 an excellent choice for low voltage precision applications with extensive temperature requirements.

The LMP7707/LMP7708/LMP7709 have only ±37 μV of typical input referred offset voltage and this offset is guaranteed to be less than ±500 μV for the single and ±520 μV for the dual and quad over temperature. This minimal offset voltage allows more accurate signal detection and amplification in precision applications.

The low input bias current of only ±200 fA along with the low input referred voltage noise of 9 nV/$\sqrt{Hz}$ give the LMP7707/LMP7708/LMP7709 superior qualities for use in sensor applications. Lower levels of noise introduced by the amplifier mean better signal fidelity and a higher signal-to-noise ratio.

The LMP7707/LMP7708/LMP7709 are stable for a gain of 6 or higher. With proper compensation though, the LMP7707, LMP7708 or LMP7709 can be operational at a gain of ±1 and still maintain much faster slew rates than comparable fully compensated amplifiers. The increase in bandwidth and slew rate is obtained without any additional power consumption.

National Semiconductor is heavily committed to precision amplifiers and the market segment they serve. Technical support and extensive characterization data is available for sensitive applications or applications with a constrained error budget.

The LMP7707 is offered in the space saving 5-Pin SOT23 package, the LMP7708 comes in the 8-pin MSOP and the LMP7709 is offered in the 14-Pin TSSOP package. These small packages are ideal solutions for area constrained PC boards and portable electronics.

CAPACITIVE LOAD

The LMP7707/LMP7708/LMP7709 devices can each be connected as a non-inverting voltage follower. This configuration is the most sensitive to capacitive loading.

The combination of a capacitive load placed on the output of an amplifier along with the amplifier's output impedance creates a phase lag which in turn reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be either underdamped or it will oscillate.

In order to drive heavier capacitive loads, an isolation resistor, R_{ISO}, as shown in the circuit in *Figure 1* should be used. By using this isolation resistor, the capacitive load is isolated from the amplifier's output, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the output voltage will be. If values of R_{ISO} are sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

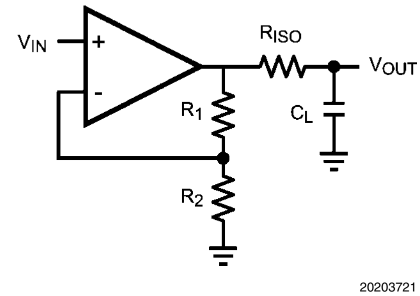


FIGURE 1. Isolating Capacitive Load

INPUT CAPACITANCE

CMOS input stages inherently have low input bias current and higher input referred voltage noise. The LMP7707/LMP7708/LMP7709 enhances this performance by having the low input bias current of only ±200 fA, as well as a very low input referred voltage noise of 9 nV/$\sqrt{Hz}$. In order to achieve this a large input stage has been used. This large input stage increases the input capacitance of the LMP7707/LMP7708/LMP7709. The typical value of this input capacitance, C_{IN}, for the LMP7707/LMP7708/LMP7709 is 25 pF. The input capacitance will interact with other impedances such as gain and feedback resistors, which are seen on the inputs of the amplifier, to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and will also cause gain peaking. In order to compensate for the input capacitance, care must be taken in choosing the feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

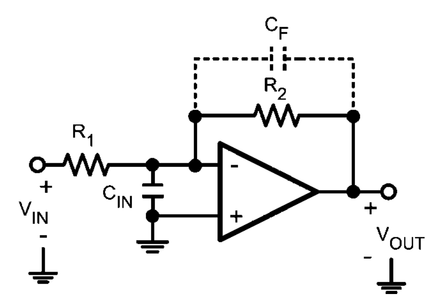


FIGURE 2. Compensating for Input Capacitance

Using this compensation method will have an impact on the high frequency gain of the op amp, due to the frequency dependent feedback of this amplifier. Low gain settings can, again, introduce instability issues.

DIODES BETWEEN THE INPUTS

The LMP7707/LMP7708/LMP7709 have a set of anti-parallel diodes between the input pins, as shown in *Figure 3*. These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than one diode voltage drop might damage the diodes. The differential signal between the inputs needs to be limited to ±300 mV or the input current needs to be limited to ±10 mA. Exceeding these limits will damage the part.

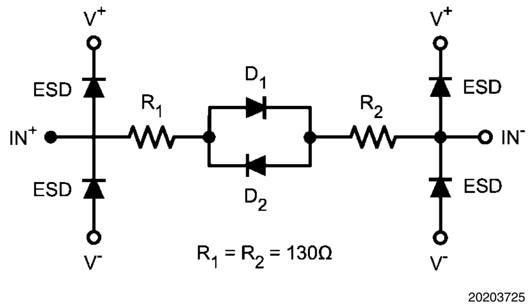


FIGURE 3. Input of the LMP7707

TOTAL NOISE CONTRIBUTION

The LMP7707/LMP7708/LMP7709 have very low input bias current, very low input current noise and very low input voltage noise. As a result, these amplifiers are ideal choices for circuits with high impedance sensor applications.

Figure 4 shows the typical input noise of the LMP7707/ LMP7708/LMP7709 as a function of source resistance. The total noise at the input can be calculated using *Equation 1*.

$$e_{ni} = \sqrt{e_n^2 + e_i^2 + e_t^2} \tag{1}$$

Where:

e_{ni} is the total noise on the input.

e_n denotes the input referred voltage noise

e_i is the voltage drop across source resistance due to input referred current noise or $e_i = R_S * i_n$

e_t is the thermal noise of the source resistance

The input current noise of the LMP7707/LMP7708/LMP7709 is so low that it will not become the dominant factor in the total noise unless source resistance exceeds 300 MΩ, which is an unrealistically high value.

As is evident in *Figure 4*, at lower R_S values, the total noise is dominated by the amplifier's input voltage noise. Once R_S is larger than a few kilo-Ohms, then the dominant noise factor becomes the thermal noise of R_S. As mentioned before, the current noise will not be the dominant noise factor for any practical application.

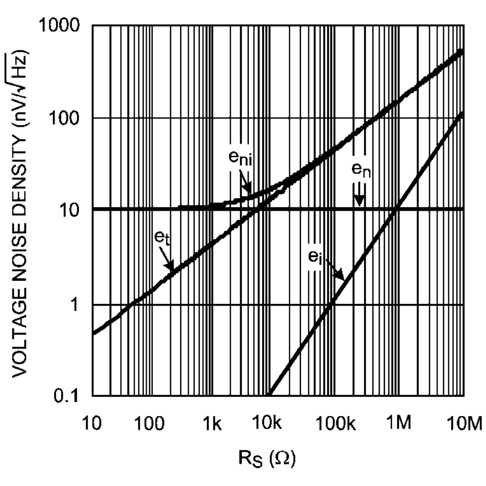


FIGURE 4. Total Input Noise

HIGH IMPEDANCE SENSOR INTERFACE

Many sensors have high source impedances that may range up to 10 MΩ. The output signal of sensors often needs to be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor's output and cause a voltage drop across the source resistance as shown in *Figure 5*, where $V_{IN}+ = V_S - I_{BIAS}*R_S$

The last term, $I_{BIAS}*R_S$, shows the voltage drop across R_S. To prevent errors introduced to the system due to this voltage, an op amp with very low input bias current must be used with high impedance sensors. This is to keep the error contribution by $I_{BIAS}*R_S$ less than the input voltage noise of the amplifier, so that it will not become the dominant noise factor. The LMP7707/LMP7708/LMP7709 have very low input bias current, typically 200 fA.

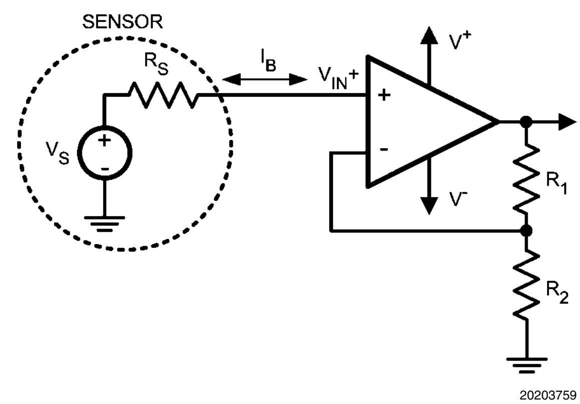


FIGURE 5. Noise Due to I_{BIAS}

USAGE OF DECOMPENSATED AMPLIFIERS

This section discusses the differences between compensated and decompensated op amps and presents the advantages of decompensated amplifiers. In high gain applications decompensated amplifiers can be used without any changes compared to standard amplifiers. However, for low gain applications special frequency compensation measures have to be taken to ensure stabilitiy.

Feedback circuit theory is discussed in detail, in particular as it applies to decompensated amplifiers. Bode plots are presented for a graphical explanation of stability analysis. Two solutions are given for creating a feedback network for decompensated amplifiers when relatively low gains are required: A simple resistive feedback network and a more advanced frequency dependent feedback network with improved noise performance. Finally, a design example is presented resulting in a practical application. The results are compared to fully compensated amplifiers (National Semiconductors LMP7701/LMP7702/LMP7704).

COMPENSATED AMPLIFIERS

A (fully) compensated op amp is designed to operate with good stability down to gains of ±1. For this reason, the compensated op amp is also called a unity gain stable op amp.

Figure 6 shows the Open Loop Response of a compensated amplifier.

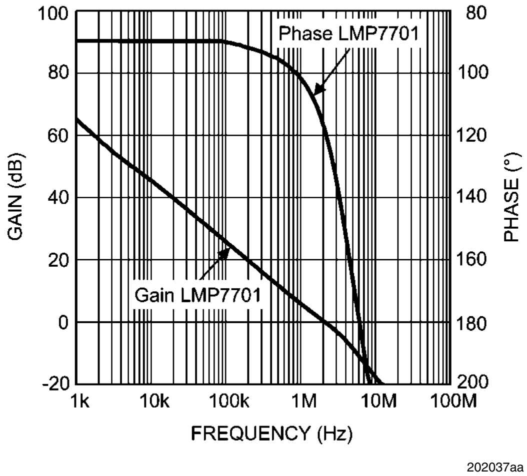


FIGURE 6. Open Loop Frequency Response Compensated Amplifier (LMP7701)

This amplifier is unity gain stable, because the phase shift is still < 180°, when the gain crosses 0 dB (unity gain).

Stability can be expressed in two different ways:

Phase Margin This is the phase difference between the actual phase shift and 180°, at the point where the gain is 0 dB.

Gain Margin This is the gain difference relative to 0 dB, at the frequency where the phase shift crosses the 180°.

The amplifier is supposed to be used with negative feedback but a phase shift of 180° will turn the negative feedback into positive feedback, resulting in oscillations. A phase shift of 180° is not a problem when the gain is smaller than 0 dB, so the critical point for stability is 180° phase shift at 0 dB gain. The gain margin and phase margin express the margin enhancing overall stability between the amplifiers response and this critical point.

DECOMPENSATED AMPLIFIERS

Decompensated amplifiers, such as the LMP7707/LMP7708/LMP7709, are designed to maximize the bandwidth and slew rate without any additional power consumption over the unity gain stable op amp. That is, a decompensated op amp has a higher bandwidth to power ratio than an equivalent compensated op amp. Compared with the unity gain stable amplifier, the decompensated version has the following advantages:

1. A wider closed loop bandwidth.
2. Better slew rate due to reduced compensation capacitance within the op amp.
3. Better Full Power Bandwidth, given with *Equation 2*.

$$FPBW = \frac{SR}{2 \pi V_P} \tag{2}$$

Figure 7 shows the frequency response of the decompensated amplifier.

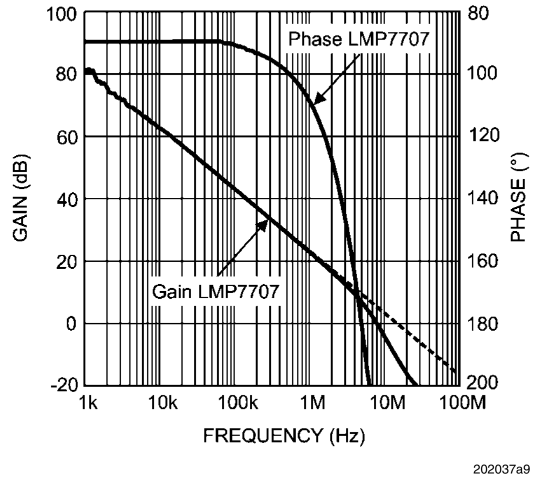


FIGURE 7. Open Loop Frequency Response Decompensated Amplifier (LMP7707)

As shown in *Figure 7*, the reduced internal compensation moves the first pole to higher frequencies. The second open loop pole for the LMP7707/LMP7708/LMP7709 occurs at 4 MHz. The extrapolated unity gain (see dashed line in *Figure 7*) occurs at 14 MHz. An ideal two pole system would give a phase margin of > 45° at the location of the second pole. Unfortunately, the LMP7707/LMP7708/LMP7709 have parasitic poles close to the second pole, giving a phase margin closer to 0°. The LMP7707/LMP7708/LMP7709 can be used at frequencies where the phase margin is > 45°. The frequency where the phase margin is 45° is at 2.4 MHz. The corresponding value of the open loop gain (also called G_{MIN}) is 6 times.

Stability has only to do with the loop gain and not with the forward gain (G) of the op amp. For high gains, the feedback network is attenuating and this reduces the loop gain; therefore the op amp will be stable for $G > G_{MIN}$ and no special measures are required. For low gains the feedback network attenuation may not be sufficient to ensure loop stability for a decompensated amplifier. However, with an external compensation network decompensated amplifiers can still be made stable while maintaining their advantages over unity gain stable amplifiers.

EXTERNAL COMPENSATION FOR GAINS LOWER THAN G_{MIN}.

This section explains how decompensated amplifiers can be used in configurations requiring a gain lower than G_{MIN}. In the next sections the concept of the feedback factor is introduced. Subsequently, an explanation is given how stability can be determined using the frequency response curve of the op amp together with the feedback factor. Using the circuit theory, it will be explained how decompensated amplifiers can be stabilized at lower gains.

FEEDBACK THEORY

Stability issues can be analyzed by verifying the loop gain function GF, where G is the open loop gain of the amplifier and F is the feedback factor of the feedback circuit.

The feedback function (F) of arbitrary electronic circuits, as shown in *Figure 8*, is defined as the ratio of the input and output signal of the same circuit.

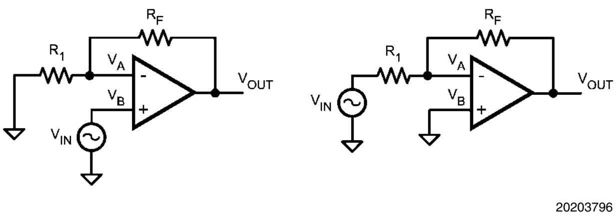


FIGURE 8. Op Amp with Resistive Feedback. (a) Non-inverting (b) Inverting

The feedback function for a three-terminal op amp as shown in *Figure 8* is the feedback voltage $V_A - V_B$ across the op amp input terminals relative to the op amp output voltage, V_{OUT}. That is

$$F = \frac{V_A - V_B}{V_{OUT}} \quad (3)$$

GRAPHICAL EXPLANATION OF STABILITY ANALYSIS

Stability issues can be observed by verifying the closed loop gain function GF. In the frequencies of interest, the open loop gain (G) of the amplifier is a number larger than 1 and therefore positive in dB. The feedback factor (F) of the feedback circuit is an attenuation and therefore negative in dB. For calculating the closed loop gain GF in dB we can add the values of G and F (both in dB).

One practical approach to stabilizing the system, is to assign a value to the feedback factor F such that the remaining loop gain GF equals one (unity gain) at the frequency of G_{MIN}. This realizes a phase margin of 45° or greater. This results in the following requirement for stability: $1/F > G_{MIN}$. The inverse feedback factor 1/F is constant over frequency and should intercept the open loop gain at a value in dB that is greater than or equal to G_{MIN}.

The inverse feedback factor for both configurations shown in *Figure 8*, is given by:

$$\frac{1}{F} = 1 + \frac{R_F}{R_1} \quad (4)$$

The closed loop gain for the non-inverting configuration (a) is:

$$A_{CL} = 1 + \frac{R_F}{R_1} = \frac{1}{F} \quad (5)$$

The closed loop gain for the inverting configuration (b) is:

$$A_{CL} = -\frac{R_F}{R_1} = 1 - \frac{1}{F} \quad (6)$$

For stable operation the phase margin must be equal to or greater than 45° . The corresponding closed loop gain G_{MIN}, for a non-inverting configuration, is

$$|A_{CL}|(\min) = G_{\min} \quad (7)$$

For an inverting configuration:

$$|A_{CL}|(\min) = G_{\min} - 1 \quad (8)$$

If R_1 and R_F and are chosen so that the closed loop gain is lower than the minimum gain required for stability, then 1/F intersects the open loop gain curve for a value that is lower than G_{MIN}. For example, assume the G_{MIN} is equal to 10 V/V (20 dB). This is shown as the dashed line in *Figure 9*. The resistor choice of $R_F = R_1 = 2\ k\Omega$ makes the inverse feedback equal 2 V/V (6 dB), shown in *Figure 9* as the solid line. The intercept of G and 1/F represents the frequency for which the loop gain is identical to 1 (0 dB). Consequently, the total phase shift at the frequency of this intercept determines the phase margin and the overall system stability. In this system example 1/F crosses the open loop gain at a frequency which is larger than the frequency where G_{MIN} occurs, therefore this system has less than 45° phase margin and is most likely instable.

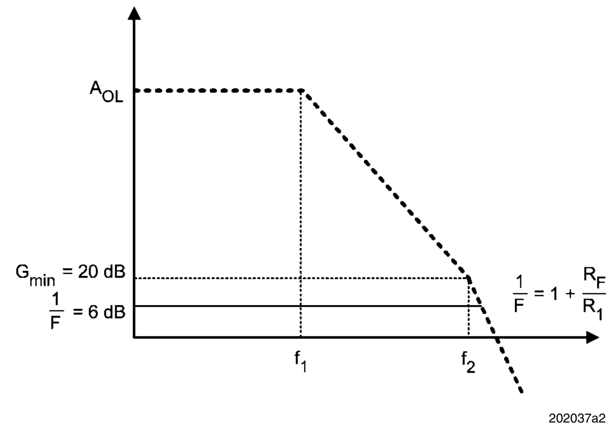


FIGURE 9. 1/F for $R_F = R_1$ and Open Loop Gain Plot

RESISTIVE COMPENSATION

A straightforward way to achieve a stable amplifier configuration is to add a resistor R_C between the inverting and the non-inverting inputs as shown in *Figure 10*.

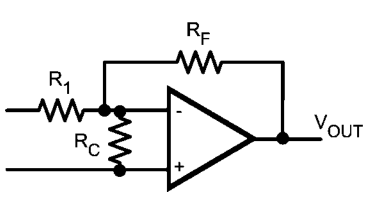


FIGURE 10. Op Amp with Compensation Resistor between Inputs

This additional resistor R_C will not affect the closed loop gain of the amplifier but it will have positive impact on the feedback network.

The inverse feedback function of this circuit is:

$$\frac{1}{F} = 1 + \frac{R_F}{R_1 // R_c} = 1 + \frac{R_F}{R_1} + \frac{R_F}{R_c} \quad (9)$$

Proper selection of the value of R_C results in the shifting of the 1/F function to G_{MIN} or greater, thus fulfilling the condition for circuit stability. The compensation technique of reducing the loop gain may be used to stabilize the circuit for the values given in the previous example, that is G_{MIN} = 20 dB and $R_F = R_1 = 2\ k\Omega$. A resistor value of 250 Ω applied between the amplifier inputs shifts the 1/F curve to the value G_{MIN} (20 dB) as shown by the dashed line in *Figure 11*. This results in overall stability for the circuit. This figure shows a combination of the open and closed loop gain and the inverse feedback function.

This example, represented by *Figure 8* and *Figure 9*, is generic in the sense that the G_{MIN} as specified did not distinguish between inverting and non-inverting configurations.

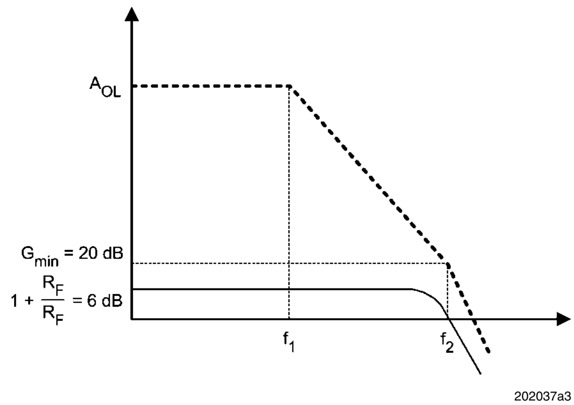


FIGURE 11. Compensation with Reduced Loop Gain

The technique of reducing loop gain to stabilize a decompensated op amp circuit will be illustrated using the non-inverting input configuration shown in *Figure 12*.

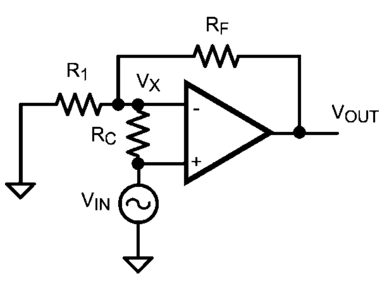


FIGURE 12. Closed Loop Gain Analysis with R_C

The effect of the choice of resistor R_C in *Figure 12* on the closed loop gain can be analyzed in the following manner:

Assume the voltage at the inverting input of the op amp is V_X. Then,

$$(V_{IN} - V_X)\, G = V_{OUT} \tag{10}$$

Where G is the open loop gain of the op amp.

$$\frac{V_X}{R_1} + \frac{V_X - V_{IN}}{R_C} = \frac{V_{OUT} - V_X}{R_F} \tag{11}$$

Combining *Equation 10*, *Equation 11*, and *Equation 9* produces the following equation for closed loop gain,

$$\frac{V_{OUT}}{V_{IN}} = \frac{1 + \frac{R_F}{R_1}}{1 + \frac{1}{GF}} \tag{12}$$

By inspection of *Equation 12*, R_C does not affect the ideal closed loop gain. In this example where $R_F = R_1$, the closed loop gain remains at 6 dB as long as GF >> 1. The closed loop gain curve is shown as the solid line in *Figure 11*.

The addition of R_C affects the circuit in the following ways:

1. 1/F is moved to a higher gain, resulting in overall system stability.

However, adding R_C results in reduced loop gain and increased noise gain. The noise gain is defined as the inverse of the feedback factor, F. The noise gain is the gain from the amplifier input referred noise to the output. In effect, loop gain is traded for stability.

2. The ideal closed loop gain retains the same value as the circuit without the compensation resistor R_C.

LEAD-LAG COMPENSATION

This section presents a more advanced compensation technique that can be used to stabilize amplifiers. The increased noise gain of the prior circuit is prevented by reducing the low frequency attenuation of the feedback circuit. This compensation method is called Lead-Lag compensation. Lead-lag compensation components will be analyzed and a design example using this procedure will be discussed.

The feedback function in a lead-lag compensation circuit is shaped using a resistor and a capacitor. They are chosen in a way that ensures sufficient phase margin.

Figure 13 shows a Bode plot containing: the open loop gain of the decompensated amplifier, a feedback function without compensation and a feedback function with lead-lag compensation.

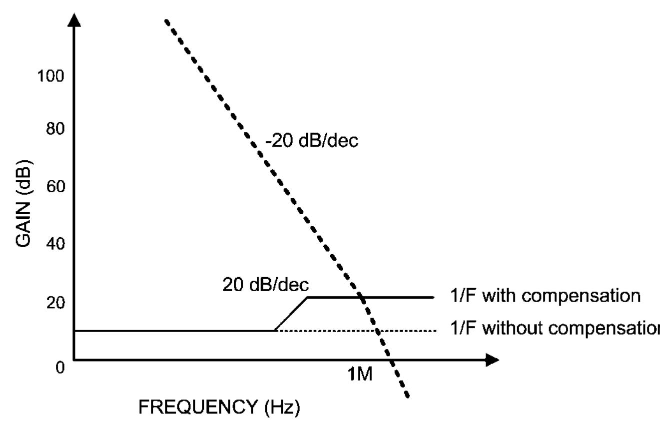


FIGURE 13. Bode Plot of Open Loop gain G and 1/F with and without Lead-Lag Compensation

The shaped feedback function presented in *Figure 13* can be realized using the amplifier configuration in *Figure 14*. Note that resistor R_P is only used for compensation of the input voltage caused by the I_{BIAS} current. R_P can be used to introduce more freedom for calculating the lead-lag components. This will be discussed later in this section.

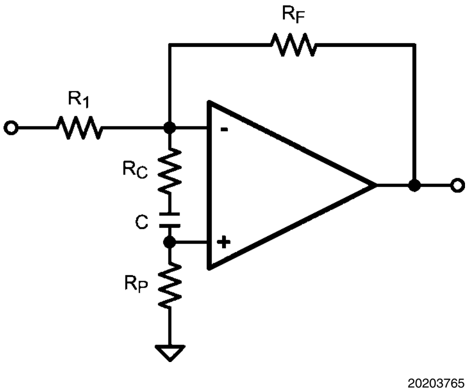


FIGURE 14. LMP7707 with Lead-Lag Compensation for Inverting Configuration

The inverse feedback factor of the circuit in *Figure 14* is:

$$\frac{1}{F} = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{1 + s(R_C + R_1//R_F + R_P)C}{1 + sR_CC}\right) \quad (13)$$

The pole of the inverse feedback function is located at:

$$f_P = \frac{1}{2\pi R_C C} \quad (14)$$

The zero of the inverse feedback function is located at:

$$f_Z = \frac{1}{2\pi(R_C + R_1//R_F + R_P)\,C} \quad (15)$$

The low frequency inverse feedback factor is given by:

$$\left.\frac{1}{F}\right|_{f=0} = 1 + \frac{R_F}{R_1} \quad (16)$$

The high frequency inverse feedback factor is given by:

$$\left.\frac{1}{F}\right|_{f=\infty} = \left(1 + \frac{R_F}{R_1}\right)\left(1 + \frac{R_P + R_1//R_F}{R_C}\right) \quad (17)$$

From these formulas, we can tell that

1. The 1/F's zero is located at a lower frequency compared to 1/F's pole.
2. The intersection point of 1/F and the open loop gain G is determined by the choice of resistor values for R_P and R_C if the values of R_1 and R_F are set before compensation.
3. This procedure results in the creation of a pole-zero pair, the positions of which are interdependent.
4. This pole-zero pair is used to:
   — Raise the 1/F value to a greater value in the region immediately to the left of its intercept with the A function in order to meet the G_{min} requirement.
   — Achieve the preceding with no additional loop phase delay.
5. The location of the 1/F zero is determined by the following conditions:
   — The value of 1/F at low frequency.
   — The value of 1/F at the intersection point.
   — The location of 1/F pole.

Note that the constraint $1/F \geq G_{min}$ needs to be satisfied only in the vicinity of the intersection of G and 1/F; 1/F can be shaped elsewhere as needed. Two rules must be satisfied in order to maintain adequate phase margin.

Rule 1 The plot of 1/F should intersect with the plot of the open loop gain at a value larger than G_{MIN}. At that point, the open loop gain G has a phase margin of 45°.

The location f_2 in *Figure 15* illustrates the proper intersection point for the LMP7707/LMP7708/LMP7709 using the circuit of *Figure 14*. The intersection of G and 1/F at the op amp's second pole location is the 45° phase margin reference point.

Rule 2 The 1/F pole (see *Figure 15*) should be positioned at the frequency that is at least one decade below the intersection point f_2 of 1/F and G. This positioning takes full advantage of the 90° of phase lead brought about by the 1/F pole. This additional phase lead accompanies the increase in magnitude of 1/F observed at frequencies greater than the 1/F pole.

The resulting system has approximately 45° of phase margin, based upon the fact that the open loop gain's dominant pole and the second pole are more than one decade apart and that the open loop gain has no other pole within one decade of its intersection point with 1/F. If there is a third pole in the open loop gain G at a frequency greater than f_2 and if it occurs less than a decade above that frequency, then there will be an effect on phase margin.

DESIGN EXAMPLE

The input lead-lag compensation method can be applied to an application using the LMP7707, LMP7708 or LMP7709 in an inverting configuration, as shown in *Figure 14*.

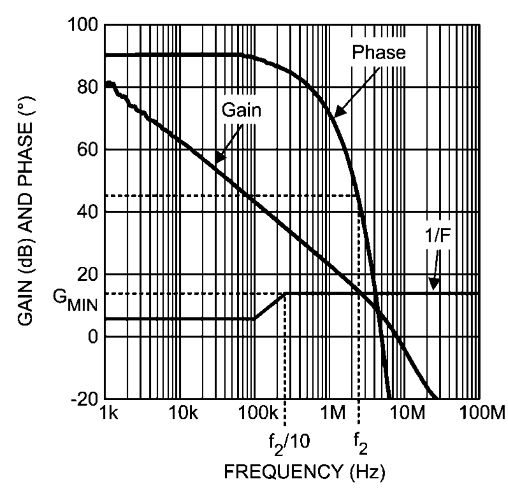


FIGURE 15. LMP7707 Open Loop Gain and 1/F Lead-Lag Feedback Network.

Figure 15 shows that G_{MIN} = 16 dB and f_2 (intersection point) = 2.4 MHz.

A gain of 6 dB (or a magnitude of –1) is well below the LMP7707's G_{MIN}. Without external lead-lag compensation, the inverse feedback factor is found using *Equation 4* which applies to both inverting and non-inverting configurations. Unity gain implementation for the inverting configuration means $R_F = R_1$, and 1/F = 2 (6 dB).

Procedure:

The compensation circuit shown in *Figure 14* is implemented. The inverse feedback function is shaped by the solid line in *Figure 15*. The 1/F plot is 6 dB at low frequencies. At higher frequencies, it is made to intersect the loop gain G at frequency f_2 with gain amplitude of 16 dB (G_{MIN}), which equals a magnitude of six times. This follows the recommendations in Rule 1. The 1/F pole f_p is set one decade below the intersection point (f_2 = 2.4 MHz) as given in Rule 2, and results in a frequency f_p = 240 kHz. The next steps should be taken to calculate the values of the compensation components:

Step 1) Set 1/F equal to G_{MIN} using *Equation 17*. This gives a value for resistor R_C.

Step 2) Set the 1/F pole one decade below the intersection point using *Equation 14*. This gives a value for capacitor C.

This method uses bode plot approximation. Some fine-tuning may be needed to get the best results.

Calculations:

As described in Step 1, use *Equation 17*.

$$\left.\frac{1}{F}\right|_{f=\infty} = \left(1 + \frac{R_F}{R_1}\right)\left(1 + \frac{R_P + R_1//R_F}{R_C}\right) = 6\ V/V \quad (18)$$

Now substitute R_F/R_1 = 1 into the equation above since this is a unity gain, inverting amplifier, then

$$R_P + R_1//R_F = 2\ R_C \quad (19)$$

According to Step 2 use *Equation 14*

$$f_P = \frac{1}{2\pi R_C C} = 240\ kHz \quad (20)$$

which leads to:

$$C = \frac{1}{2\pi f R_C} \quad (21)$$

Choose a value of R_F that is below 2 kΩ, in order to minimize the possibility of shunt capacitance across high value resistors producing a negative effect on high frequency operation. If $R_F = R_1$ = 1 kΩ, then R_F // R_1 = 500 Ω. For simplicity, choose R_P = 0 Ω . The value of R_C is derived from *Equation 19* and has a value of R_C = 250 Ω. This is not a standard value. A value of R_C = 330 Ω is a first choice (using 10% tolerance components).

The value of capacitor C is 2.2 nF. This value is significantly higher than the parasitic capacitances associated with passive components and board layout, and is therefore a good solution.

Bench results:

For bench evaluation the LMP7707 in an inverting configuration has been verified under three different conditions:

- Uncompensated.
- Lead-lag compensation resulting in a phase margin of 45°.
- Lead lag overcompensation resulting in a phase margin larger than 45°.

The calculated components for these three conditions are

Condition	R_C	C
Uncompensated	NA	NA
Compensated	330 Ω	2.2 nF
Overcompensated	240 Ω	3.3 nF

Figure 16 shows the results of the compensation of the LMP7707.

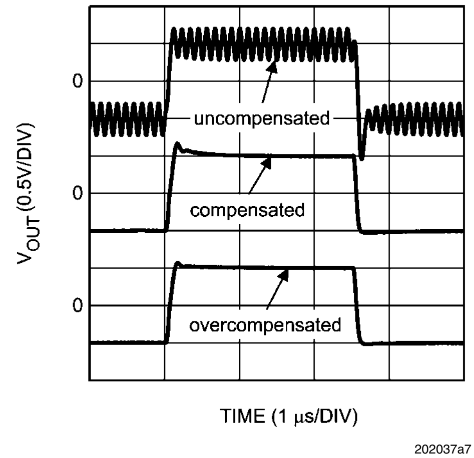


FIGURE 16. Bench Results for Lead- Lag Compensation

The top waveform shows the output response of a uncompensated LMP7707 using no external compensation components. This trace shows ringing and is unstable (as expected). The middle waveform is the response of a compensated LMP7707 using the compensation components calculated with the described procedure. The response is reasonably well behaved. The bottom waveform shows the response of an overcompensated LMP7707.

Finally, *Figure 17* compares the step response of the compensated LMP7707 to that of the unity gain stable LMP7701. The increase in dynamic performance is clear.

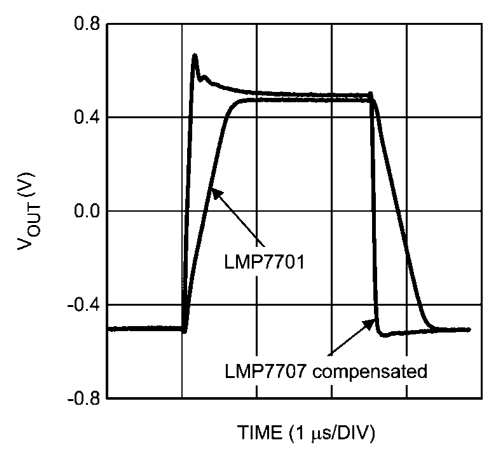
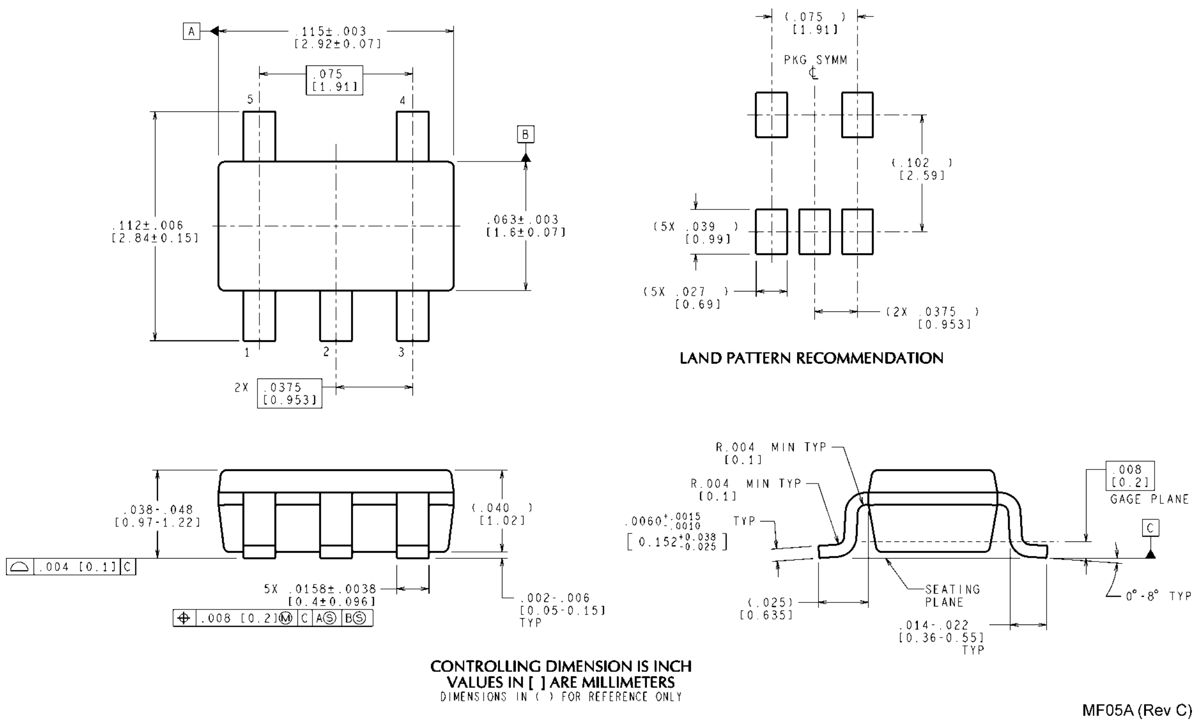


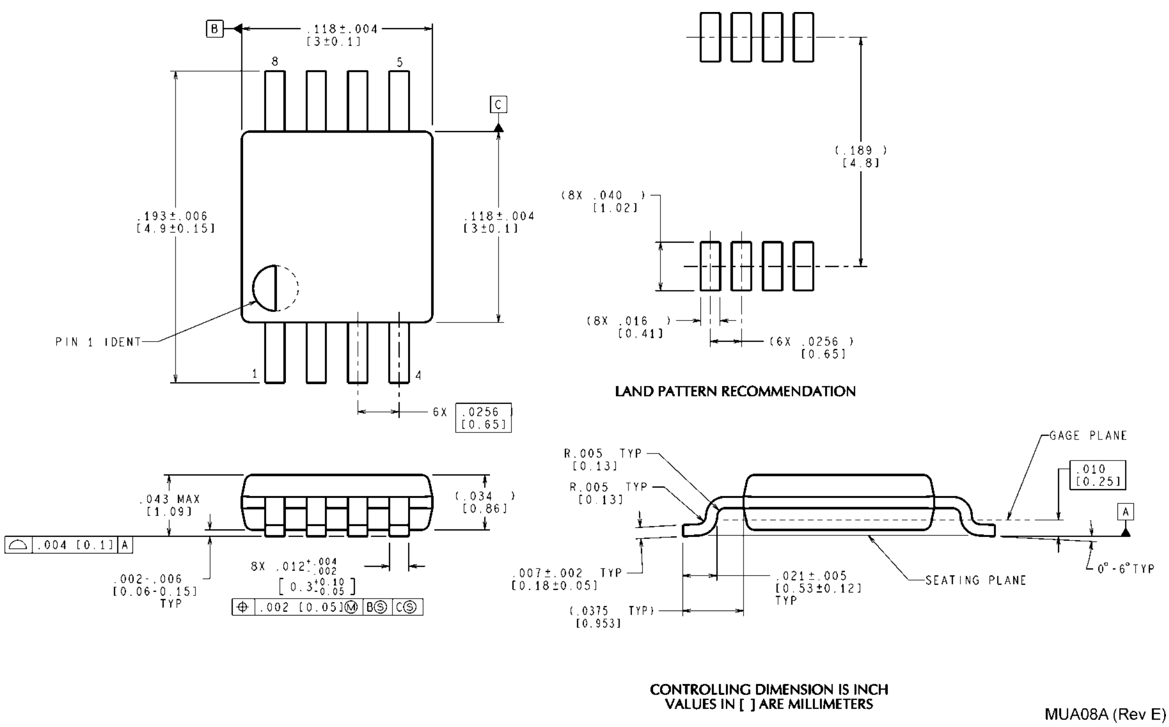
FIGURE 17. Bench Results for Comparison of LMP7701 and LMP7707

The application of input lead-lag compensation to a decompensated op amp enables the realization of circuit gains of less than the minimum specified by the manufacturer. This is accomplished while retaining the advantageous speed versus power characteristic of decompensated op amps.

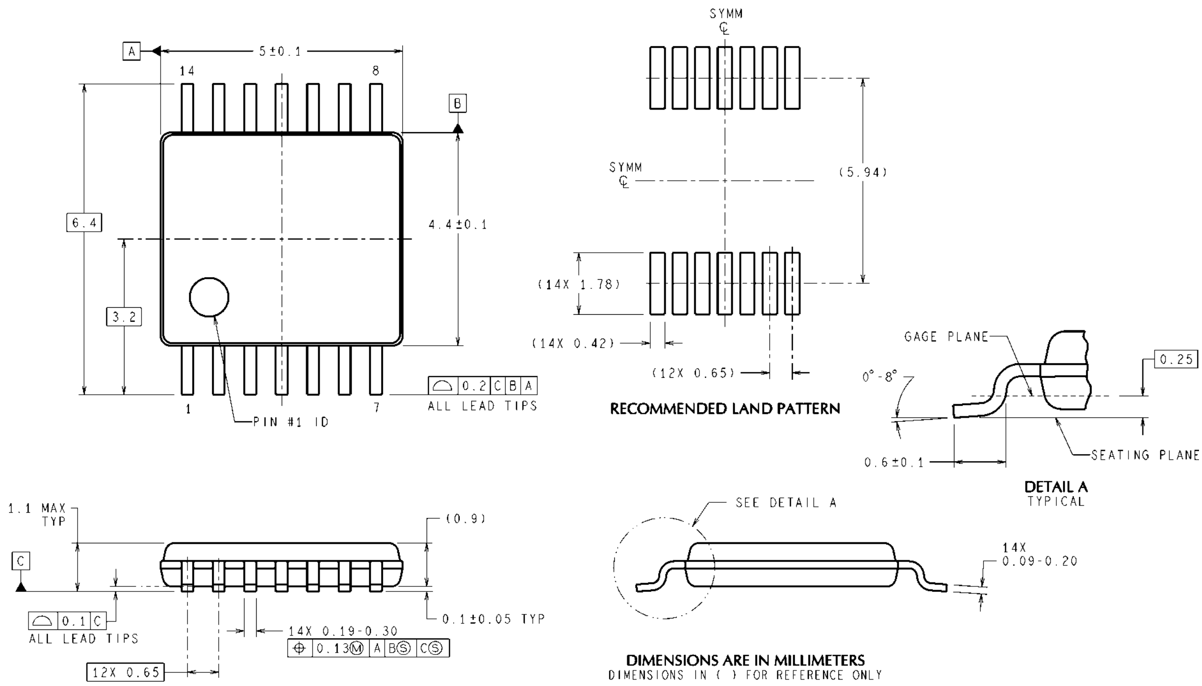
Physical Dimensions inches (millimeters) unless otherwise noted



5-Pin SOT23
NS Package Number MF05A



8-Pin MSOP
NS Package Number MUA08A



MTC14 (Rev D)

14-Pin TSSOP
NS Package Number MTC14

Notes

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