# NEC

**MOS INTEGRATED CIRCUIT**

# $\mu$**PD75P0076**

## 4-BIT SINGLE-CHIP MICROCONTROLLER

The $\mu$PD75P0076 replaces the $\mu$PD750068's internal mask ROM with a one-time PROM and features expanded ROM capacity.

Because the $\mu$PD75P0076 supports programming by users, it is suitable for use in prototype testing for system development using the $\mu$PD750064, 750066, and 750068 products, and for use in small-lot production.

**Detailed information about function is provided in the following user's manual.**
**Be sure to read it before designing:**
$\mu$**PD750068 User's Manual: U10670E**

### FEATURES
○ Compatible with $\mu$PD750068
○ Memory capacity:
  • PROM : 16384 x 8 bits
  • RAM : 512 x 4 bits
○ Can operate with same power supply voltage as the mask ROM version $\mu$PD750068
  $V_{DD}$ = 1.8 to 5.5 V
○ On-chip A/D converter capable of low-voltage operation ($AV_{REF}$ = 1.8 to 5.5 V)
  8-bit resolution x 8 channels
○ Small shrink SOP package

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| $\mu$PD75P0076CU | 42-pin plastic shrink DIP (600 mil, 1.778-mm pitch) |
| $\mu$PD75P0076GT | 42-pin plastic shrink SOP (375 mil, 0.8-mm pitch) |

**Caution   On-chip pull-up resistors by mask option cannot be provided.**

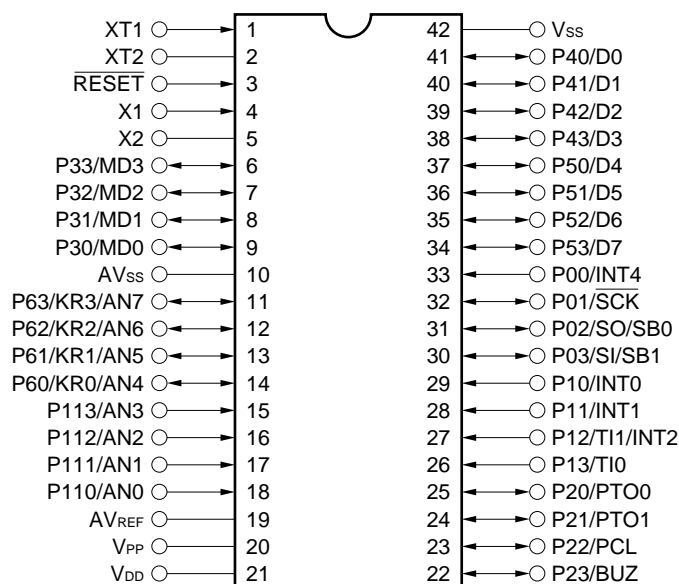The information in this document is subject to change without notice.

**The mark ★ shows major revised points.**

**Functional Outline**

| Parameter | | Function |
|---|---|---|
| Instruction execution time | | • 0.95, 1.91, 3.81, 15.3 μs (@ 4.19 MHz with main system clock)<br>• 0.67, 1.33, 2.67, 10.7 μs (@ 6.0 MHz with main system clock)<br>• 122 μs (@ 32.768 kHz with subsystem clock) |
| On-chip memory | PROM | 16384 x 8 bits |
| | RAM | 512 x 4 bits |
| General-purpose register | | • 4-bit operation:  8 x 4 banks<br>• 8-bit operation:  4 x 4 banks |
| Input/output port | CMOS input | 12 | Connections of on-chip pull-up resistors can be specified by software:  7<br>Also used for analog input pins:  4 |
| | CMOS input/output | 12 | Connections of on-chip pull-up resistors can be specified by software:  12<br>Also used for analog input pins:  4 |
| | N-ch open-drain input/output pins | 8 | 13-V withstand voltage |
| | Total | 32 | |
| Timer | | 4 channels<br>• 8-bit timer/event counter:  2 channels (can be used as the 16-bit timer/event counter)<br>• 8-bit basic interval timer/watchdog timer:  1 channel<br>• Watch timer:  1 channel |
| Serial interface | | • 3-wire serial I/O mode ⋯ MSB or LSB can be selected for transferring first bit<br>• 2-wire serial I/O mode |
| A/D converter | | 8-bit resolution x 8 channels (1.8 V ≤ AV$_{REF}$ ≤ V$_{DD}$) |
| Bit sequential buffer | | 16 bits |
| Clock output (PCL) | | • Φ, 1.05 MHz, 262 kHz, 65.5 kHz (@ 4.19 MHz with main system clock)<br>• Φ, 1.5 MHz, 375 kHz, 93.8 kHz (@ 6.0 MHz with main system clock) |
| Buzzer output (BUZ) | | • 2, 4, 32 kHz  (@ 4.19 MHz with main system clock  or<br>                              @ 32.768 kHz with subsystem clock)<br>• 2.93, 5.86, 46.9 kHz (@ 6.0 MHz with main system clock) |
| Vectored interrupts | | External: 3, Internal: 4 |
| Test input | | External: 1, Internal: 1 |
| System clock oscillator | | • Ceramic or crystal oscillator for main system clock oscillation<br>• Crystal oscillator for subsystem clock oscillation |
| Standby function | | STOP/HALT mode |
| Operating ambient temperature | | T$_A$ = −40 to +85 ˚C |
| Power supply voltage | | V$_{DD}$ = 1.8 to 5.5 V |
| Package | | • 42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)<br>• 42-pin plastic shrink SOP (375 mil, 0.8-mm pitch) |

## CONTENTS

## 1. PIN CONFIGURATION (Top View)

- **42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)**
  $\mu$**PD75P0076CU**
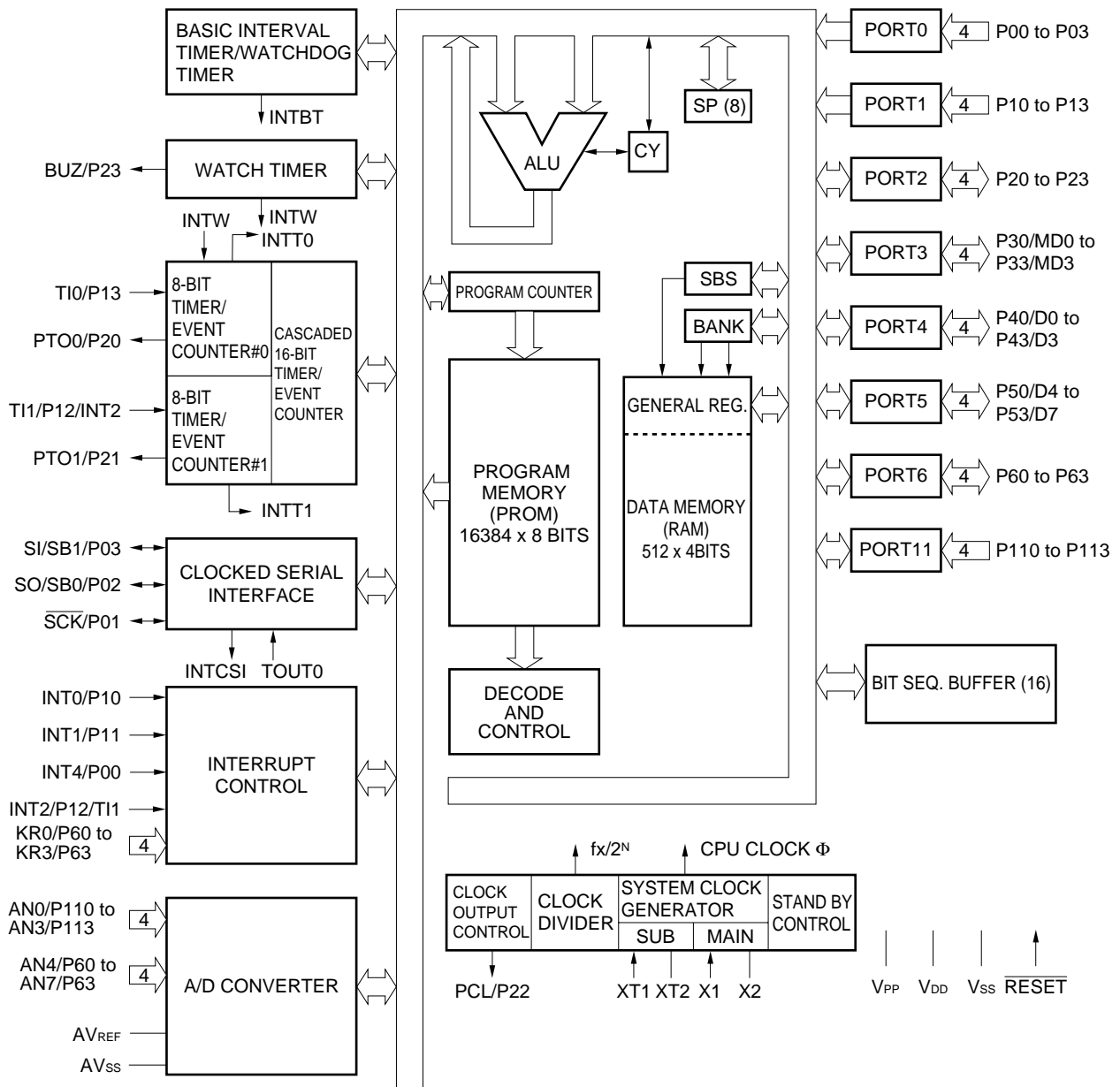- **42-pin plastic shrink SOP (375 mil, 0.8-mm pitch)**
  $\mu$**PD75P0076GT**

| | | | |
|---|---|---|---|
| XT1 | 1 | 42 | Vss |
| XT2 | 2 | 41 | P40/D0 |
| RESET | 3 | 40 | P41/D1 |
| X1 | 4 | 39 | P42/D2 |
| X2 | 5 | 38 | P43/D3 |
| P33/MD3 | 6 | 37 | P50/D4 |
| P32/MD2 | 7 | 36 | P51/D5 |
| P31/MD1 | 8 | 35 | P52/D6 |
| P30/MD0 | 9 | 34 | P53/D7 |
| AVss | 10 | 33 | P00/INT4 |
| P63/KR3/AN7 | 11 | 32 | P01/SCK |
| P62/KR2/AN6 | 12 | 31 | P02/SO/SB0 |
| P61/KR1/AN5 | 13 | 30 | P03/SI/SB1 |
| P60/KR0/AN4 | 14 | 29 | P10/INT0 |
| P113/AN3 | 15 | 28 | P11/INT1 |
| P112/AN2 | 16 | 27 | P12/TI1/INT2 |
| P111/AN1 | 17 | 26 | P13/TI0 |
| P110/AN0 | 18 | 25 | P20/PTO0 |
| AVREF | 19 | 24 | P21/PTO1 |
| VPP | 20 | 23 | P22/PCL |
| VDD | 21 | 22 | P23/BUZ |

In normal operation mode, make sure to connect VPP directly to VDD.

### Pin Identification

| | | | |
|---|---|---|---|
| AN0 to AN7 | : Analog Input 0 to 7 | P110 to P113 | : Port 11 |
| AVREF | : Analog Reference | PCL | : Programmable Clock |
| AVss | : Analog Ground | PTO0, PTO1 | : Programmable Timer Output 0, 1 |
| BUZ | : Buzzer Clock | RESET | : Reset Input |
| D0 to D7 | : Data Bus 0 to 7 | SB0, SB1 | : Serial Data Bus 0, 1 |
| INT0, INT1, INT4 | : External Vectored Interrupt 0, 1, 4 | SCK | : Serial Clock |
| INT2 | : External Test Input 2 | SI | : Serial Input |
| KR0 to KR3 | : Key Return | SO | : Serial Output |
| MD0 to MD3 | : Mode Selection 0 to 3 | TI0, TI1 | : Timer Input 0, 1 |
| P00 to P03 | : Port 0 | VDD | : Positive Power Supply |
| P10 to P13 | : Port 1 | VPP | : Programmable Power Supply |
| P20 to P23 | : Port 2 | Vss | : Ground |
| P30 to P33 | : Port 3 | X1, X2 | : Main System Clock Oscillation 1, 2 |
| P40 to P43 | : Port 4 | XT1, XT2 | : Subsystem Clock Oscillation 1, 2 |
| P50 to P53 | : Port 5 | | |
| P60 to P63 | : Port 6 | | |

## 2. BLOCK DIAGRAM

BASIC INTERVAL TIMER/WATCHDOG TIMER
INTBT
WATCH TIMER — BUZ/P23
INTW      INTW
         INTT0
8-BIT TIMER/ EVENT COUNTER#0 — TI0/P13, PTO0/P20
CASCADED 16-BIT TIMER/ EVENT COUNTER
8-BIT TIMER/ EVENT COUNTER#1 — TI1/P12/INT2, PTO1/P21
INTT1

CLOCKED SERIAL INTERFACE — SI/SB1/P03, SO/SB0/P02, SCK/P01
INTCSI   TOUT0

INTERRUPT CONTROL — INT0/P10, INT1/P11, INT4/P00, INT2/P12/TI1, KR0/P60 to KR3/P63 [4]

A/D CONVERTER — AN0/P110 to AN3/P113 [4], AN4/P60 to AN7/P63 [4], AVREF, AVSS

ALU      CY      SP (8)

PROGRAM COUNTER

SBS
BANK

PROGRAM MEMORY (PROM) 16384 x 8 BITS

GENERAL REG.
DATA MEMORY (RAM) 512 x 4BITS

DECODE AND CONTROL

PORT0 [4] P00 to P03
PORT1 [4] P10 to P13
PORT2 [4] P20 to P23
PORT3 [4] P30/MD0 to P33/MD3
PORT4 [4] P40/D0 to P43/D3
PORT5 [4] P50/D4 to P53/D7
PORT6 [4] P60 to P63
PORT11 [4] P110 to P113

BIT SEQ. BUFFER (16)

fx/2$^N$      CPU CLOCK $\Phi$

CLOCK OUTPUT CONTROL | CLOCK DIVIDER | SYSTEM CLOCK GENERATOR (SUB | MAIN) | STAND BY CONTROL

PCL/P22      XT1 XT2 X1  X2      V$_{PP}$  V$_{DD}$  V$_{SS}$  RESET

## 3. PIN FUNCTIONS

### 3.1 Port Pins

| Pin name | I/O | Alternate function | Function | 8-bit accessible | After reset | I/O circuit type[Note 1] |
|---|---|---|---|---|---|---|
| P00 | I | INT4 | This is a 4-bit input port (PORT0). For P01 to P03, on-chip pull-up resistors are software-specifiable in 3-bit units. | Not available | Input | \<B\> |
| P01 | I/O | $\overline{\text{SCK}}$ | | | | \<F\>-A |
| P02 | I/O | SO/SB0 | | | | \<F\>-B |
| P03 | I/O | SI/SB1 | | | | \<M\>-C |
| P10 | I | INT0 | This is a 4-bit input port (PORT1). Connections of on-chip pull-up resistors are software-specifiable in 4-bit units. P10/INT0 can select a noise elimination circuit. | Not available | Input | \<B\>-C |
| P11 | | INT1 | | | | |
| P12 | | TI1/INT2 | | | | |
| P13 | | TI0 | | | | |
| P20 | I/O | PTO0 | This is a 4-bit I/O port (PORT2). Connections of on-chip pull-up resistors are software-specifiable in 4-bit units. | Not available | Input | E-B |
| P21 | | PTO1 | | | | |
| P22 | | PCL | | | | |
| P23 | | BUZ | | | | |
| P30 | I/O | MD0 | This is a programmable 4-bit I/O port (PORT3). Input and output can be specified in single-bit units. Connections of on-chip pull-up resistors are software-specifiable in 4-bit units. | Not available | Input | E-B |
| P31 | | MD1 | | | | |
| P32 | | MD2 | | | | |
| P33 | | MD3 | | | | |
| ★ P40[Note 2] | I/O | D0 | This is an N-ch open-drain 4-bit I/O port (PORT4). In the open-drain mode, withstands up to 13 V. Also used as data I/O pin (lower 4 bits) for program memory (PROM) write/verify. | Available | High impedance | M-E |
| P41[Note 2] | | D1 | | | | |
| P42[Note 2] | | D2 | | | | |
| P43[Note 2] | | D3 | | | | |
| ★ P50[Note 2] | I/O | D4 | This is an N-ch open-drain 4-bit I/O port (PORT5). In the open-drain mode, withstands up to 13 V. Also used as data I/O pin (upper 4 bits) for program memory (PROM) write/verify. | | High impedance | M-E |
| P51[Note 2] | | D5 | | | | |
| P52[Note 2] | | D6 | | | | |
| P53[Note 2] | | D7 | | | | |
| P60 | I/O | KR0/AN4 | This is a programmable 4-bit I/O port (PORT6). Input and output can be specified in single-bit units. Connections of on-chip pull-up resistors are software-specifiable in 4-bit units. | Not available | Input | \<Y\>-D |
| P61 | | KR1/AN5 | | | | |
| P62 | | KR2/AN6 | | | | |
| P63 | | KR3/AN7 | | | | |
| P110 | I | AN0 | This is a 4-bit input port (PORT11). | Not available | Input | Y-A |
| P111 | | AN1 | | | | |
| P112 | | AN2 | | | | |
| P113 | | AN3 | | | | |

**Notes 1.** Circuit types enclosed in brackets indicate Schmitt triggered inputs.

**2.** Low-level input current leakage increases when input instructions or bit manipulation instructions are executed.

**3.2 Non-port Pins (1/2)**

| Pin name | I/O | Alternate function | Function | | After reset | Circuit type^Note |
|---|---|---|---|---|---|---|
| TI0 | I | P13 | Inputs external event pulses to the timer/event counter. | | Input | <B>-C |
| TI1 | | P12/INT2 | | | | |
| PTO0 | O | P20 | Timer/event counter output | | Input | E-B |
| PTO1 | | P21 | | | | |
| PCL | | P22 | Clock output | | | |
| BUZ | | P23 | Optional frequency output (for buzzer output or system clock trimming) | | | |
| $\overline{SCK}$ | I/O | P01 | Serial clock I/O | | Input | <F>-A |
| SO/SB0 | | P02 | Serial data output Serial data bus I/O | | | <F>-B |
| SI/SB1 | | P03 | Serial data input Serial data bus I/O | | | <M>-C |
| INT4 | I | P00 | Edge detection vectored interrupt input (both rising edge and falling edge detection) | | | <B> |
| INT0 | I | P10 | Edge detection vectored interrupt input (detection edge can be selected). INT0/P10 can select a noise eliminator. | Noise eliminator/ asynchronous selection | Input | <B>-C |
| INT1 | | P11 | | Asynchronous | | |
| INT2 | | P12/TI1 | Rising edge detection testable input | Asynchronous | | |
| KR0 to KR3 | I | P60/AN4 to P63/AN7 | Falling edge detection testable input | | Input | <Y>-D |
| AN0 to AN3 | I | P110 to P113 | Analog signal input | | Input | Y-A |
| AN4 to AN7 | | P60/KR0 to P63/KR3 | | | | <Y>-D |
| AV$_{REF}$ | — | — | A/D converter reference voltage | | — | Z-N |
| AV$_{SS}$ | — | — | A/D converter reference GND potential | | — | Z-N |
| X1 | I | — | Crystal/ceramic connection pin for the main system clock oscillator. When inputting the external clock, input the external clock to pin X1, and the inverted phase of the external clock to pin X2. | | — | — |
| X2 | — | | | | | |
| XT1 | I | — | Crystal connection pin for the subsystem clock oscillator. When the external clock is used, input the external clock to pin XT1, and the inverted phase of the external clock to pin XT2. Pin XT1 can be used as a 1-bit input (test) pin. | | — | — |
| XT2 | — | | | | | |
| $\overline{RESET}$ | I | — | System reset input (low-level active) | | — | <B> |

**Note**  Circuit types enclosed in brackets indicate Schmitt triggered inputs.
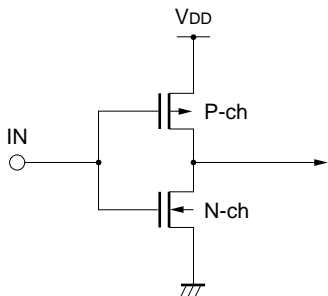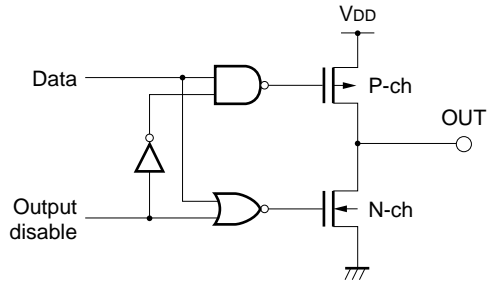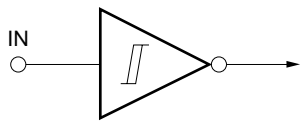
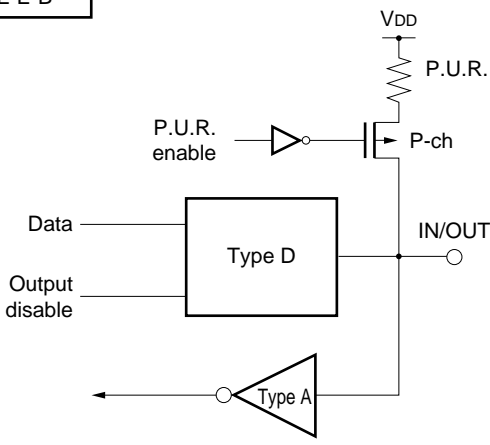★

### 3.2 Non-port Pins (2/2)
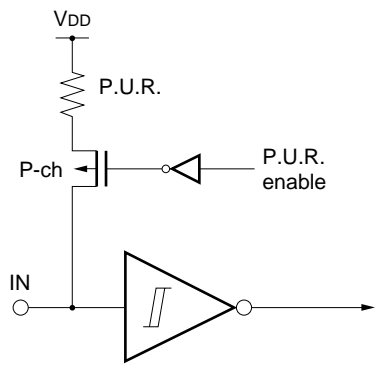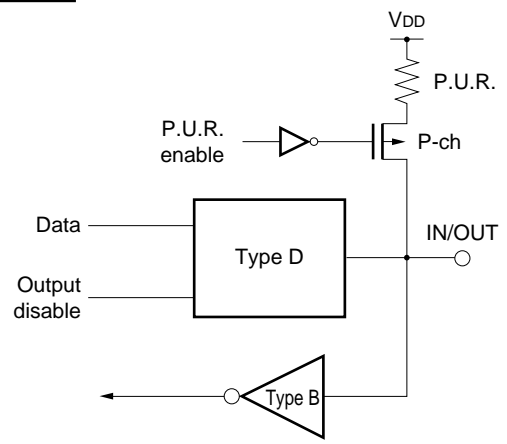
| Pin name | I/O | Alternate function | Function | After reset | Circuit type |
|---|---|---|---|---|---|
| MD0 to MD3 | I | P30 to 33 | Mode selection for program memory (PROM) write/verify. | Input | E-B |
| D0 to D3 | I/O | P40 to 43 | Data bus pin for program memory (PROM) write/verify. | Input | M-E |
| D4 to D7 | | P50 to 53 | | | |
| $V_{PP}$**Note** | — | — | Programmable voltage supply in program memory (PROM) write/verify mode. In normal operation mode, connect directly to $V_{DD}$. Apply +12.5 V in PROM write/verify mode. | — | — |
| $V_{DD}$ | — | — | Positive power supply | — | — |
| $V_{SS}$ | — | — | Ground | — | — |

**Note** During normal operation, the $V_{PP}$ pin will not operate normally unless connected to $V_{DD}$ pin.
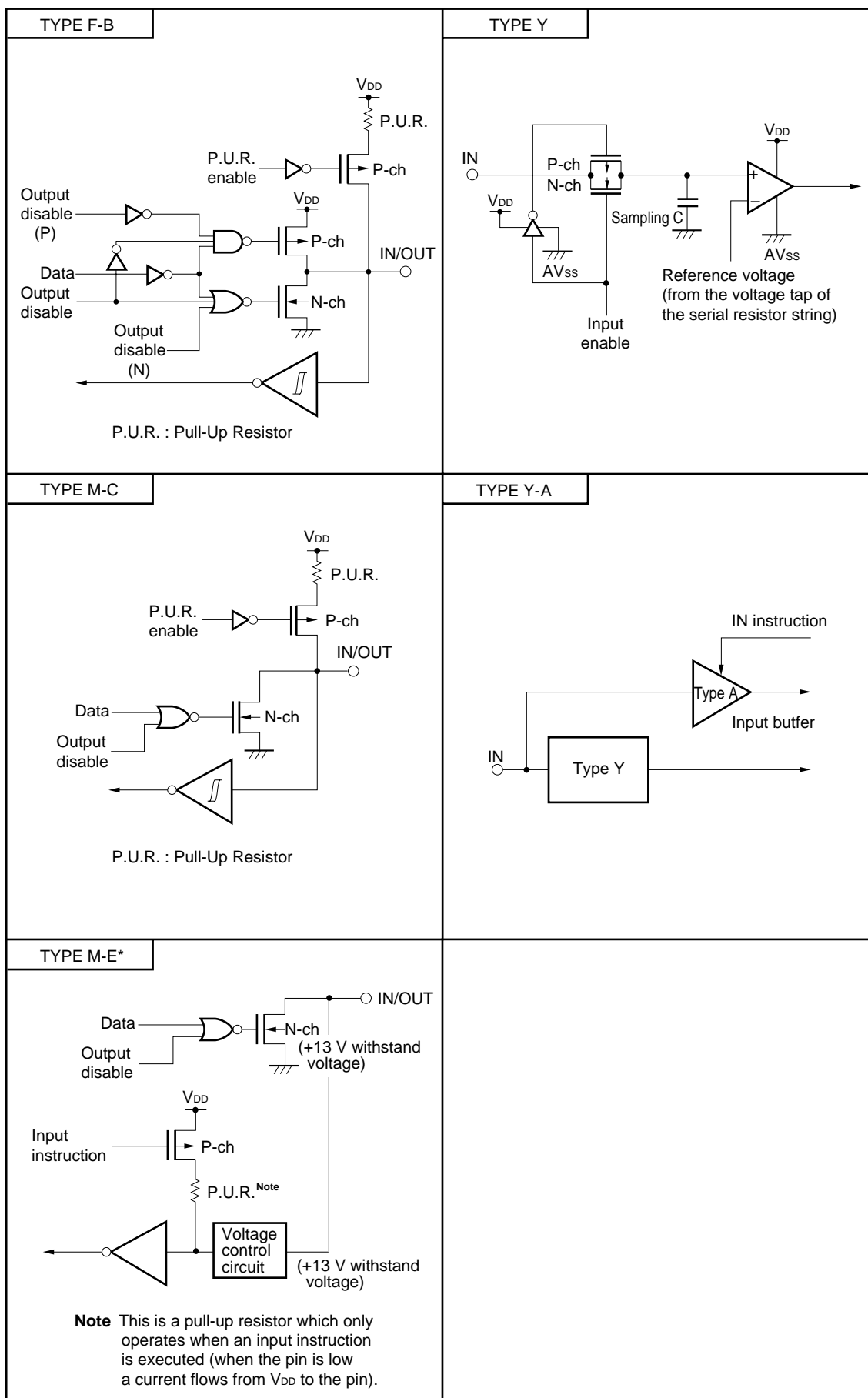
### 3.3 Equivalent Circuits for Pins

The equivalent circuits for the $\mu$PD75P0076's pin are shown in schematic diagrams below.
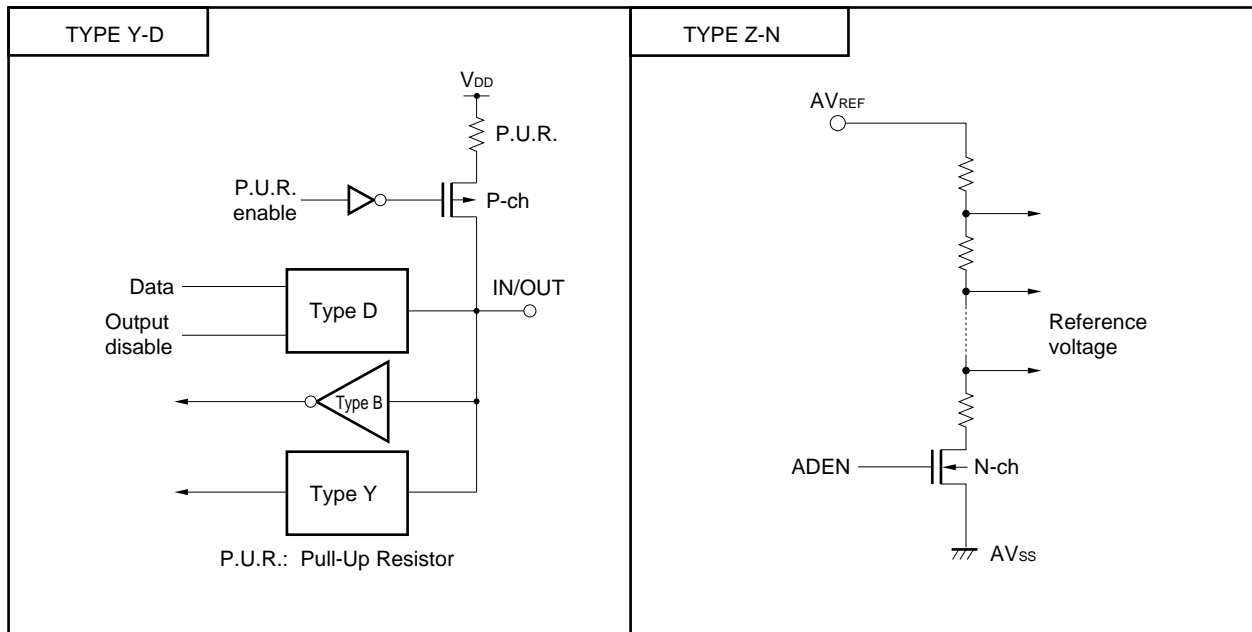
(1/3)



TYPE A

CMOS standard input buffer

TYPE D

Push-pull output that can be set to high impedance output (with both P-ch and N-ch OFF).

TYPE B

Schmitt trigger input with hysteresis characteristics.

TYPE E-B

P.U.R. : Pull-Up Resistor

TYPE B-C

P.U.R. : Pull-Up Resistor

Schmitt trigger input with hysteresis characteristics.

TYPE F-A

P.U.R. : Pull-Up Resistor

### TYPE F-B

V_DD

P.U.R.

P.U.R. enable

P-ch

Output disable (P)

V_DD

P-ch

Data

IN/OUT

Output disable

N-ch

Output disable (N)

P.U.R. : Pull-Up Resistor

### TYPE Y

IN

P-ch
N-ch

V_DD

V_DD

Sampling C

+
−

Input enable

AV_SS

AV_SS

Reference voltage (from the voltage tap of the serial resistor string)

### TYPE M-C

V_DD

P.U.R.

P.U.R. enable

P-ch

IN/OUT

Data

N-ch

Output disable

P.U.R. : Pull-Up Resistor

### TYPE Y-A

IN instruction

Type A

Input butfer

IN

Type Y

### TYPE M-E*

IN/OUT

Data

N-ch (+13 V withstand voltage)

Output disable

V_DD

Input instruction

P-ch

P.U.R.**Note**

Voltage control circuit

(+13 V withstand voltage)

**Note** This is a pull-up resistor which only operates when an input instruction is executed (when the pin is low a current flows from V_DD to the pin).

**10**

TYPE Y-D

$V_{DD}$

P.U.R.

P.U.R. enable

P-ch

Data

Output disable

Type D

IN/OUT

Type B

Type Y

P.U.R.: Pull-Up Resistor

TYPE Z-N

$AV_{REF}$

Reference voltage

ADEN

N-ch

$AV_{SS}$

★ **3.4 Handling of Unused Pins**

| Pin | Recommended connection |
|---|---|
| P00/INT4 | Connect to $V_{SS}$ or $V_{DD}$ |
| P01/$\overline{SCK}$ | Independently connect to $V_{SS}$ or $V_{DD}$ through resistor |
| P02/SO/SB0 | |
| P03/SI/SB1 | Connected to $V_{SS}$ |
| P10/INT0, P11/INT1 | Connect to $V_{SS}$ or $V_{DD}$ |
| P12/TI1/INT2 | |
| P13/TI0 | |
| P20/PTO0 | Input mode : independently connected to $V_{SS}$ or $V_{DD}$ through resistor |
| P21/PTO1 | |
| P22/PCL | Output mode : open |
| P23/BUZ | |
| P30/MD0 to P33/MD3 | |
| P40/D0 to P43/D3 | Connected to $V_{SS}$ |
| P50/D4 to P53/D7 | |
| P60/KR0/AN4 to P63/KR3/AN7 | Input mode : independently connected to $V_{SS}$ or $V_{DD}$ through resistor<br>Output mode : open |
| P110/AN0 to P113/AN3 | Connected to $V_{SS}$ or $V_{DD}$ |
| XT1**Note** | Connect to $V_{SS}$ or $V_{DD}$ |
| XT2**Note** | Open |
| $V_{PP}$ | Make sure to connect directly to $V_{DD}$ |
| $AV_{REF}$ | Connect to $V_{SS}$ |
| $AV_{SS}$ | |

**Note** When the subsystem clock is not used, set SOS.0 = 1 (on-chip feedback resistor is not used).

## 4.  SWITCHING  BETWEEN  Mk  I  AND  Mk  II  MODES

Setting a stack bank selection (SBS) register for the $\mu$PD75P0076 enables the program memory to be switched between the Mk I mode and the Mk II mode.  This capability enables the evaluation of the $\mu$PD750064, 750066,  and 750068 using the $\mu$PD75P0076.

When the SBS bit 3 is set to 1:  sets Mk I mode (corresponds to Mk I mode of $\mu$PD750064, 750066, and 750068)
When the SBS bit 3 is set to 0:  sets Mk II mode (corresponds to Mk II mode of $\mu$PD750064, 750066, and 750068)

### 4.1  Differences between Mk I Mode and Mk II Mode

Table 4-1 lists the differences between the Mk I mode and the Mk II mode of the $\mu$PD75P0076.

**Table 4-1.  Differences between Mk I Mode and Mk II Mode**

| Item | | Mk I Mode | Mk II Mode |
|---|---|---|---|
| Program counter | | $PC_{13\ to\ 0}$ | |
| Program memory (bytes) | | 16384 | |
| Data memory (bits) | | 512 x 4 | |
| Stack | Stack bank | Selectable from memory banks 0 and 1 | |
| | Stack bytes | 2 bytes | 3 bytes |
| Instruction | BRA !addr1 CALLA !addr1 | Not provided | Provided |
| Instruction execution time | CALL !addr | 3 machine cycles | 4 machine cycles |
| | CALLF !faddr | 2 machine cycles | 3 machine cycles |
| Supported mask ROM versions and mode | | Mk I mode of $\mu$PD750064, 750066, and 750068 | Mk II mode of $\mu$PD750064, 750066, and 750068 |

★      **Caution**  **The Mk II mode supports a program area which exceeds 16K bytes in the 75X and 75XL series.  This mode enhances the software compatibility with products which have more than 16K bytes.**
**When the Mk II mode is selected, the number of stack bytes used in execution of a subroutine call instruction increases by 1 per stack for the usable area compared to the Mk I mode.  Furthermore, when a CALL !addr, or CALLF !faddr instruction is used, each instruction takes another machine cycle. Therefore, when more importance is attached to RAM utilization or throughput than software compatibility, use the Mk I mode.**
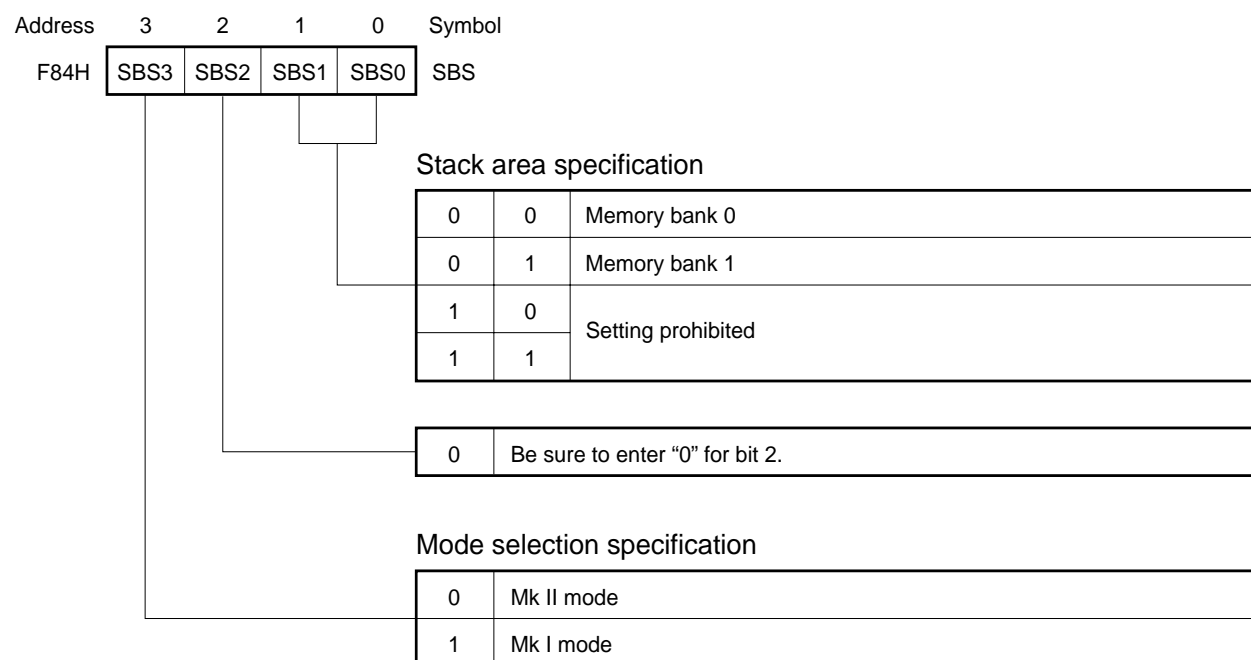
**4.2  Setting of Stack Bank Selection (SBS) Register**

Use the stack bank selection register to switch between the Mk I mode and the Mk II mode.  Figure 4-1 shows the format for doing this.

The stack bank selection register is set using a 4-bit memory manipulation instruction.  When using the Mk I mode, be sure to initialize the stack bank selection register to 100xB**Note** at the beginning of the program.  When using the Mk II mode, be sure to initialize it to 000xB**Note**.

**Note**   Set the desired value for x.

**Figure 4-1.  Format of Stack Bank Selection Register**

| Address | 3 | 2 | 1 | 0 | Symbol |
|---------|------|------|------|------|--------|
| F84H | SBS3 | SBS2 | SBS1 | SBS0 | SBS |

Stack area specification

| | | |
|---|---|---|
| 0 | 0 | Memory bank 0 |
| 0 | 1 | Memory bank 1 |
| 1 | 0 | Setting prohibited |
| 1 | 1 | |

| | |
|---|---|
| 0 | Be sure to enter "0" for bit 2. |

Mode selection specification

| | |
|---|---|
| 0 | Mk II mode |
| 1 | Mk I mode |

**Cautions 1.  SBS3 is set to "1" after $\overline{\text{RESET}}$ input, and consequently the CPU operates in the Mk I mode.  When using instructions for the Mk II mode, set SBS3 to "0" to enter the Mk II mode before using the instructions.**

**2.  When using the Mk II mode, execute a subroutine call instruction and an interrupt instruction after $\overline{\text{RESET}}$ input and after setting the stack bank selection register.**

## 5. DIFFERENCES BETWEEN $\mu$PD75P0076 AND $\mu$PD750064, 750066 AND 750068

The $\mu$PD75P0076 replaces the internal mask ROM in the $\mu$PD750064, 750066, and 750068 with a one-time PROM and features expanded ROM capacity.  The $\mu$PD75P0076's Mk I mode supports the Mk I mode in the $\mu$PD750064, 750066, and 750068 and the $\mu$PD75P0076's Mk II mode supports the Mk II mode in the $\mu$PD750064, 750066, and 750068.
Table 5-1 lists differences among the $\mu$PD75P0076 and the $\mu$PD750064, 750066, 750068.  Be sure to check the differences between corresponding versions beforehand, especially when a PROM version is used for debugging or prototype testing of application systems and later the corresponding mask ROM version is used for full-scale production. For further description of CPU functions and internal hardware, see the $\mu$**PD750064 and 750068 Preliminary Product Information (U10165E)**.

★                         **Table 5-1.  Differences between $\mu$PD75P0076 and $\mu$PD750064, 750066, 750068**

| Item | | $\mu$PD750064 | $\mu$PD750066 | $\mu$PD750068 | $\mu$PD75P0076 |
|---|---|---|---|---|---|
| Program counter | | 12-bit | | 13-bit | 14-bit |
| Program memory (bytes) | | Mask ROM 4096 | Mask ROM 6144 | Mask ROM 8192 | One-time PROM 16384 |
| Data memory (x 4 bits) | | 512 | | | |
| Mask options | Pull-up resistor for ports 4 and 5 | Yes (on-chip specifiable) | | | No (off chip) |
| | Wait time when RESET | Yes ($2^{17}$/f$_X$, $2^{15}$/f$_X$ selectable)**Note** | | | No (fixed at $2^{15}$/f$_X$)**Note** |
| | Feedback resistor of subsystem clock | Yes (Use/not use selectable) | | | No (Use) |
| Pin configuration | Pins 6 to 9 | P33 to P30 | | | P33/MD3 to P30/MD0 |
| | Pin 20 | IC | | | V$_{PP}$ |
| | Pins 34 to 37 | P53 to P50 | | | P53/D7 to P53/D4 |
| | Pins 38 to 41 | P43 to P40 | | | P43/D3 to P40/D0 |
| Other | | Noise resistance and noise radiation may differ due to different circuit complexities and mask layouts. | | | |

**Note** $2^{17}$/f$_X$ is 21.8 ms in 6.0 MHz operation and 31.3 ms in 4.19 MHz operation.
      $2^{15}$/f$_X$ is 5.46 ms in 6.0 MHz operation and 7.81 ms in 4.19 MHz operation.

**Caution   Noise resistance and noise radiation are different in PROM version and mask ROM versions.  If using a mask ROM version instead of the PROM version for processes between prototype development and full production, be sure to fully evaluate the CS of the mask ROM version (not ES).**
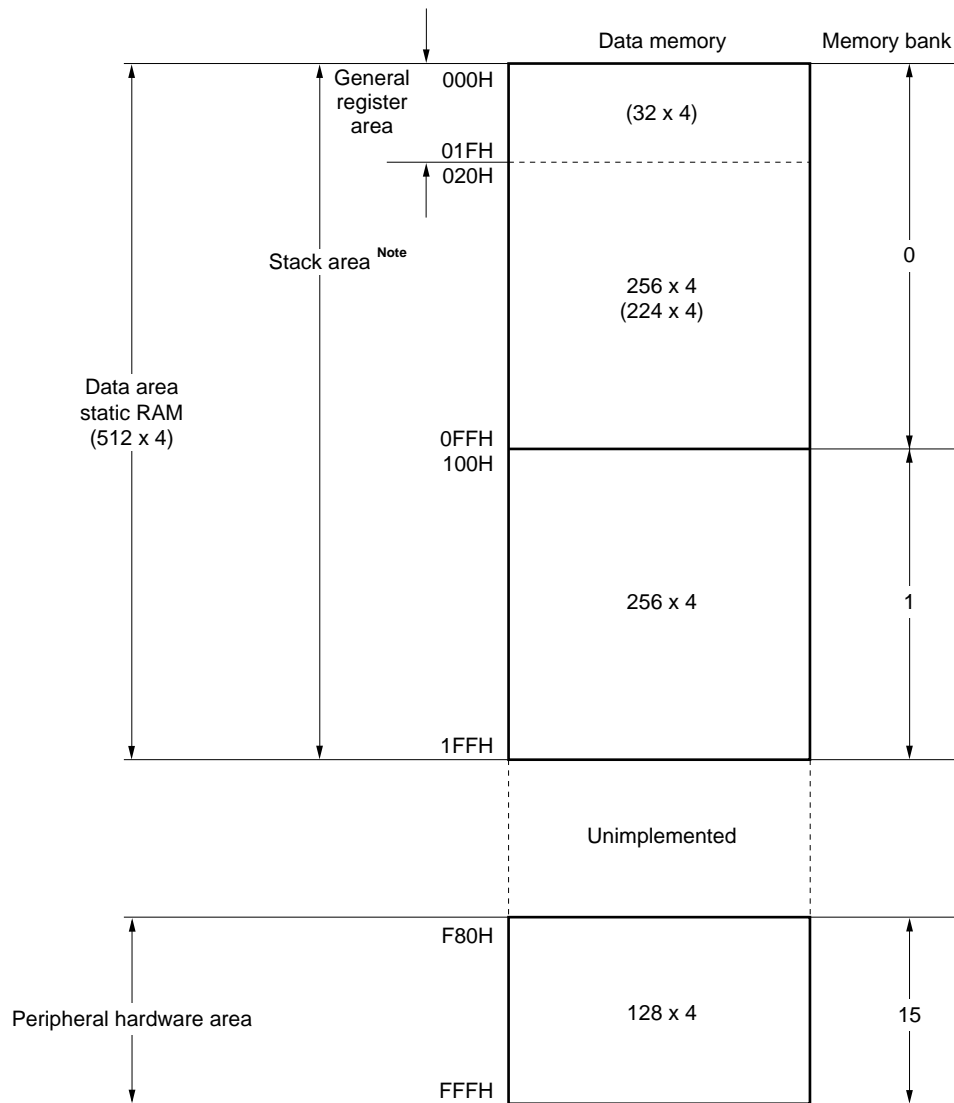
## 6. MEMORY CONFIGURATION

**Figure 6-1. Program Memory Map**
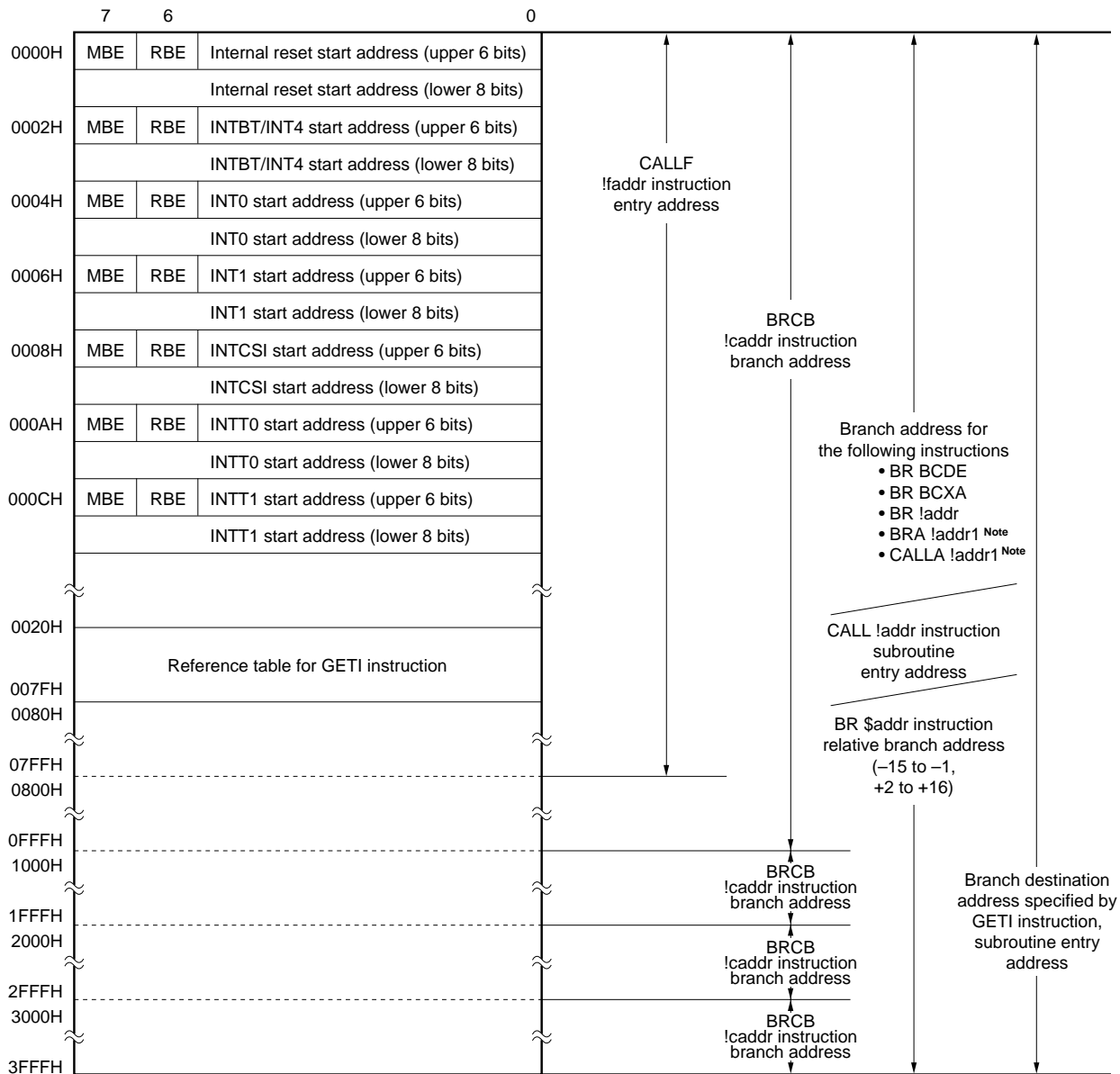


★ **Note** Can be used only in Mk II mode.

**Remark** For instructions other than those noted above, the "BR PCDE" and "BR PCXA" instructions can be used to branch to addresses with changes in the PC's lower 8 bits only.

**Figure 6-2.  Data Memory Map**



**Note**   Either memory bank 0 or 1 can be selected as the stack area.

### 7. INSTRUCTION SET

**(1) Representation and coding formats for operands**

In the instruction's operand area, use the following coding format to describe operands corresponding to the instruction's operand representations (for further description, see the **RA75X Assembler Package User's Manual–Language (EEU-1363)**). When there are several codes, select and use just one. Uppercase letters, and + and – symbols are key words that should be entered as they are.

For immediate data, enter an appropriate numerical value or label.

Instead of mem, fmem, pmem, bit, etc., a register flag symbol can be described as a label descriptor (for further description, see the $\mu$**PD750068 User's Manual (U10670E)**). Labels that can be entered for fmem and pmem are restricted.

| Representation | Coding format |
|---|---|
| reg | X, A, B, C, D, E, H, L |
| reg1 | X, B, C, D, E, H, L |
| rp | XA, BC, DE, HL |
| rp1 | BC, DE, HL |
| rp2 | BC, DE |
| rp' | XA, BC, DE, HL, XA', BC', DE', HL' |
| rp'1 | BC, DE, HL, XA', BC', DE', HL' |
| rpa | HL, HL+, HL–, DE, DL |
| rpa1 | DE, DL |
| n4 | 4-bit immediate data or label |
| n8 | 8-bit immediate data or label |
| mem | 8-bit immediate data or label[Note] |
| bit | 2-bit immediate data or label |
| fmem | FB0H to FBFH, FF0H to FFFH immediate data or label |
| pmem | FC0H to FFFH immediate data or label |
| addr | 0000H to 3FFFH immediate data or label |
| addr1 | 000H to 3FFFH immediate data or label (in Mk II mode only) |
| caddr | 12-bit immediate data or label |
| faddr | 11-bit immediate data or label |
| taddr | 20H to 7FH immediate data (however, bit0 = 0) or label |
| PORTn | PORT0 to PORT6, PORT11 |
| IEXXX | IEBT, IECSI, IET0, IET1, IE0 to IE2, IE4, IEW |
| RBn | RB0 to RB3 |
| MBn | MB0, MB1, MB15 |

**Note** When processing 8-bit data, only even addresses can be specified.

**(2) Operation legend**

| | |
|---|---|
| A | : A register; 4-bit accumulator |
| B | : B register |
| C | : C register |
| D | : D register |
| E | : E register |
| H | : H register |
| L | : L register |
| X | : X register |
| XA | : Register pair (XA); 8-bit accumulator |
| BC | : Register pair (BC) |
| DE | : Register pair (DE) |
| HL | : Register pair (HL) |
| XA' | : Expansion register pair (XA') |
| BC' | : Expansion register pair (BC') |
| DE' | : Expansion register pair (DE') |
| HL' | : Expansion register pair (HL') |
| PC | : Program counter |
| SP | : Stack pointer |
| CY | : Carry flag; bit accumulator |
| PSW | : Program status word |
| MBE | : Memory bank enable flag |
| RBE | : Register bank enable flag |
| PORTn | : Port n (n = 0 to 6, 11) |
| IME | : Interrupt master enable flag |
| IPS | : Interrupt priority select register |
| IExxx | : Interrupt enable flag |
| RBS | : Register bank select register |
| MBS | : Memory bank select register |
| PCC | : Processor clock control register |
| . | : Delimiter for address and bit |
| (xx) | : Contents of address xx |
| xxH | : Hexadecimal data |

**(3) Description of symbols used in addressing area**

| | | |
|---|---|---|
| *1 | MB = MBE • MBS<br><br>      MBS = 0, 1, 15 | |
| *2 | MB = 0 | |
| *3 | MBE = 0    : MB = 0 (000H to 07FH)<br><br>              MB = 15 (F80H to FFFH)<br><br>MBE = 1    : MB = MBS<br><br>              MBS = 0, 1, 15 | Data memory addressing |
| *4 | MB = 15, fmem = FB0H to FBFH, FF0H to FFFH | |
| *5 | MB = 15, pmem = FC0H to FFFH | |
| *6 | addr = 0000H to 3FFFH | |
| *7 | addr, addr1 = (Current PC) −15 to (Current PC) −1<br><br>             (Current PC) +2 to (Current PC) +16 | |
| *8 | caddr = 0000H to 0FFFH ($PC_{13,\,12}$ = 00B) or<br><br>         1000H to 1FFFH ($PC_{13,\,12}$ = 01B) or<br><br>         2000H to 2FFFH ($PC_{13,\,12}$ = 10B) or<br><br>         3000H to 3FFFH ($PC_{13,\,12}$ = 11B) | Program memory addressing |
| *9 | faddr = 0000H to 07FFH | |
| *10 | taddr = 0020H to 007FH | |
| *11 | addr1 = 0000H to 3FFFH (Mk II mode only) | |

**Remarks 1.** MB indicates access-enabled memory banks.

        **2.** In area *2, MB = 0 for both MBE and MBS.

        **3.** In areas *4 and *5, MB = 15 for both MBE and MBS.

        **4.** Areas *6 to *11 indicate corresponding address-enabled areas.

**(4) Description of machine cycles**

S indicates the number of machine cycles required for skipping of skip-specified instructions.  The value of S varies as shown below.

    • No skip ........................................................................ S = 0
    • Skipped instruction is 1-byte or 2-byte instruction ......... S = 1
    • Skipped instruction is 3-byte instruction**Note** ................... S = 2

    **Note**  3-byte instructions:  BR !addr, BRA !addr1, CALL !addr, CALLA !addr1

    **Caution    The GETI instruction is skipped for one machine cycle.**

One machine cycle equals one cycle (= $t_{CY}$) of the CPU clock $\Phi$.  Use the PCC setting to select among four cycle times.

| Group | Mnemonic | Operand | No. of bytes | Machine cycle | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Transfer | MOV | A, #n4 | 1 | 1 | A ← n4 | | String-effect A |
| | | reg1, #n4 | 2 | 2 | reg1 ← n4 | | |
| | | XA, #n8 | 2 | 2 | XA ← n8 | | String-effect A |
| | | HL, #n8 | 2 | 2 | HL ← n8 | | String-effect B |
| | | rp2, #n8 | 2 | 2 | rp2 ← n8 | | |
| | | A, @HL | 1 | 1 | A ← (HL) | *1 | |
| | | A, @HL+ | 1 | 2 + S | A ← (HL), then L ← L + 1 | *1 | L = 0 |
| | | A, @HL− | 1 | 2 + S | A ← (HL), then L ← L − 1 | *1 | L = FH |
| | | A, @rpa1 | 1 | 1 | A ← (rpa1) | *2 | |
| | | XA, @HL | 2 | 2 | XA ← (HL) | *1 | |
| | | @HL, A | 1 | 1 | (HL) ← A | *1 | |
| | | @HL, XA | 2 | 2 | (HL) ← XA | *1 | |
| | | A, mem | 2 | 2 | A ← (mem) | *3 | |
| | | XA, mem | 2 | 2 | XA ← (mem) | *3 | |
| | | mem, A | 2 | 2 | (mem) ← A | *3 | |
| | | mem, XA | 2 | 2 | (mem) ← XA | *3 | |
| | | A, reg1 | 2 | 2 | A ← reg1 | | |
| | | XA, rp' | 2 | 2 | XA ← rp' | | |
| | | reg1, A | 2 | 2 | reg1 ← A | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← XA | | |
| | XCH | A, @HL | 1 | 1 | A ↔ (HL) | *1 | |
| | | A, @HL+ | 1 | 2 + S | A ↔ (HL), then L ← L + 1 | *1 | L = 0 |
| | | A, @HL− | 1 | 2 + S | A ↔ (HL), then L ← L − 1 | *1 | L = FH |
| | | A, @rpa1 | 1 | 1 | A ↔ (rpa1) | *2 | |
| | | XA, @HL | 2 | 2 | XA ↔ (HL) | *1 | |
| | | A, mem | 2 | 2 | A ↔ (mem) | *3 | |
| | | XA, mem | 2 | 2 | XA ↔ (mem) | *3 | |
| | | A, reg1 | 1 | 1 | A ↔ reg1 | | |
| | | XA, rp' | 2 | 2 | XA ↔ rp' | | |
| Table reference | MOVT | XA, @PCDE | 1 | 3 | XA ← (PC$_{13-8}$ + DE)$_{ROM}$ | | |
| | | XA, @PCXA | 1 | 3 | XA ← (PC$_{13-8}$ + XA)$_{ROM}$ | | |
| | | XA, @BCDE | 1 | 3 | XA ← (BCDE)$_{ROM}$**Note** | *11 | |
| | | XA, @BCXA | 1 | 3 | XA ← (BCXA)$_{ROM}$**Note** | *11 | |

**Note**   As for the B register, only the lower 2 bits are valid.

| Group | Mnemonic | Operand | No. of bytes | Machine cycle | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Bit transfer | MOV1 | CY, fmem.bit | 2 | 2 | CY ← (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H + mem.bit | 2 | 2 | CY ← (H + mem$_{3-0}$.bit) | *1 | |
| | | fmem.bit, CY | 2 | 2 | (fmem.bit) ← CY | *4 | |
| | | pmem.@L, CY | 2 | 2 | (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← CY | *5 | |
| | | @H + mem.bit, CY | 2 | 2 | (H + mem$_{3-0}$.bit) ← CY | *1 | |
| Operation | ADDS | A, #n4 | 1 | 1 + S | A ← A + n4 | | carry |
| | | XA, #n8 | 2 | 2 + S | XA ← XA + n8 | | carry |
| | | A, @HL | 1 | 1 + S | A ← A + (HL) | *1 | carry |
| | | XA, rp' | 2 | 2 + S | XA ← XA + rp' | | carry |
| | | rp'1, XA | 2 | 2 + S | rp'1 ← rp'1 + XA | | carry |
| | ADDC | A, @HL | 1 | 1 | A, CY ← A + (HL) + CY | *1 | |
| | | XA, rp' | 2 | 2 | XA, CY ← XA + rp' + CY | | |
| | | rp'1, XA | 2 | 2 | rp'1, CY ← rp'1 + XA + CY | | |
| | SUBS | A, @HL | 1 | 1 + S | A ← A – (HL) | *1 | borrow |
| | | XA, rp' | 2 | 2 + S | XA ← XA – rp' | | borrow |
| | | rp'1, XA | 2 | 2 + S | rp'1 ← rp'1 – XA | | borrow |
| | SUBC | A, @HL | 1 | 1 | A, CY ← A – (HL) – CY | *1 | |
| | | XA, rp' | 2 | 2 | XA, CY ← XA – rp' – CY | | |
| | | rp'1, XA | 2 | 2 | rp'1, CY ← rp'1 – XA – CY | | |
| | AND | A, #n4 | 2 | 2 | A ← A∧n4 | | |
| | | A, @HL | 1 | 1 | A ← A∧(HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA∧rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1∧XA | | |
| | OR | A, #n4 | 2 | 2 | A ← A∨n4 | | |
| | | A, @HL | 1 | 1 | A ← A∨(HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA∨rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1∨XA | | |
| | XOR | A, #n4 | 2 | 2 | A ← A∀n4 | | |
| | | A, @HL | 1 | 1 | A ← A∀(HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA∀rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1∀XA | | |

| Group | Mnemonic | Operand | No. of bytes | Machine cycle | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Accumulator manipulate | RORC | A | 1 | 1 | $CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$ | | |
| | NOT | A | 2 | 2 | $A \leftarrow \overline{A}$ | | |
| Increment/ decrement | INCS | reg | 1 | 1 + S | $reg \leftarrow reg + 1$ | | reg = 0 |
| | | rp1 | 1 | 1 + S | $rp1 \leftarrow rp1 + 1$ | | rp1 = 00H |
| | | @HL | 2 | 2 + S | $(HL) \leftarrow (HL) + 1$ | *1 | (HL) = 0 |
| | | mem | 2 | 2 + S | $(mem) \leftarrow (mem) + 1$ | *3 | (mem) = 0 |
| | DECS | reg | 1 | 1 + S | $reg \leftarrow reg - 1$ | | reg = FH |
| | | rp' | 2 | 2 + S | $rp' \leftarrow rp' - 1$ | | rp' = FFH |
| Compare | SKE | reg, #n4 | 2 | 2 + S | Skip if reg = n4 | | reg = n4 |
| | | @HL, #n4 | 2 | 2 + S | Skip if (HL) = n4 | *1 | (HL) = n4 |
| | | A, @HL | 1 | 1 + S | Skip if A = (HL) | *1 | A = (HL) |
| | | XA, @HL | 2 | 2 + S | Skip if XA = (HL) | *1 | XA = (HL) |
| | | A, reg | 2 | 2 + S | Skip if A = reg | | A = reg |
| | | XA, rp' | 2 | 2 + S | Skip if XA = rp' | | XA = rp' |
| Carry flag manipulate | SET1 | CY | 1 | 1 | $CY \leftarrow 1$ | | |
| | CLR1 | CY | 1 | 1 | $CY \leftarrow 0$ | | |
| | SKT | CY | 1 | 1 + S | Skip if CY = 1 | | CY = 1 |
| | NOT1 | CY | 1 | 1 | $CY \leftarrow \overline{CY}$ | | |

| Group | Mnemonic | Operand | No. of bytes | Machine cycle | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Memory bit manipulate | SET1 | mem.bit | 2 | 2 | (mem.bit) ← 1 | *3 | |
| | | fmem.bit | 2 | 2 | (fmem.bit) ← 1 | *4 | |
| | | pmem.@L | 2 | 2 | (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 1 | *5 | |
| | | @H + mem.bit | 2 | 2 | (H + mem$_{3-0}$.bit) ← 1 | *1 | |
| | CLR1 | mem.bit | 2 | 2 | (mem.bit) ← 0 | *3 | |
| | | fmem.bit | 2 | 2 | (fmem.bit) ← 0 | *4 | |
| | | pmem.@L | 2 | 2 | (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 0 | *5 | |
| | | @H + mem.bit | 2 | 2 | (H + mem$_{3-0}$.bit) ← 0 | *1 | |
| | SKT | mem.bit | 2 | 2 + S | Skip if(mem.bit) = 1 | *3 | (mem.bit) = 1 |
| | | fmem.bit | 2 | 2 + S | Skip if(fmem.bit) = 1 | *4 | (fmem.bit) = 1 |
| | | pmem.@L | 2 | 2 + S | Skip if(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 1 | *5 | (pmem.@L) = 1 |
| | | @H + mem.bit | 2 | 2 + S | Skip if(H + mem$_{3-0}$.bit) = 1 | *1 | (@H+mem.bit) = 1 |
| | SKF | mem.bit | 2 | 2 + S | Skip if(mem.bit) = 0 | *3 | (mem.bit) = 0 |
| | | fmem.bit | 2 | 2 + S | Skip if(fmem.bit) = 0 | *4 | (fmem.bit) = 0 |
| | | pmem.@L | 2 | 2 + S | Skip if(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 0 | *5 | (pmem.@L) = 0 |
| | | @H + mem.bit | 2 | 2 + S | Skip if(H + mem$_{3-0}$.bit) = 0 | *1 | (@H+mem.bit) = 0 |
| | SKTCLR | fmem.bit | 2 | 2 + S | Skip if(fmem.bit) = 1 and clear | *4 | (fmem.bit) = 1 |
| | | pmem.@L | 2 | 2 + S | Skip if(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 1 and clear | *5 | (pmem.@L) = 1 |
| | | @H + mem.bit | 2 | 2 + S | Skip if(H + mem$_{3-0}$.bit) = 1 and clear | *1 | (@H+mem.bit) = 1 |
| | AND1 | CY, fmem.bit | 2 | 2 | CY ← CY∧(fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY∧(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H + mem.bit | 2 | 2 | CY ← CY∧(H + mem$_{3-0}$.bit) | *1 | |
| | OR1 | CY, fmem.bit | 2 | 2 | CY ← CY∨(fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY∨(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H + mem.bit | 2 | 2 | CY ← CY∨(H + mem$_{3-0}$.bit) | *1 | |
| | XOR1 | CY, fmem.bit | 2 | 2 | CY ← CY∀(fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY∀(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H + mem.bit | 2 | 2 | CY ← CY∀(H + mem$_{3-0}$.bit) | *1 | |

| Group | Mnemonic | Operand | No. of bytes | Machine cycle | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Branch | BR[Note 1] | addr | — | — | $PC_{13-0} \leftarrow$ addr<br>Assembler selects the most appropriate instruction among the following:<br>• BR !addr<br>• BRCB !caddr<br>• BR \$addr | *6 | |
| | | addr1 | — | — | $PC_{13-0} \leftarrow$ addr1<br>Assembler selects the most appropriate instruction among the following:<br>• BRA !addr1<br>• BR !addr<br>• BRCB !caddr<br>• BR \$addr1 | *11 | |
| | | !addr | 3 | 3 | $PC_{13-0} \leftarrow$ addr | *6 | |
| | | \$addr | 1 | 2 | $PC_{13-0} \leftarrow$ addr | *7 | |
| | | \$addr1 | 1 | 2 | $PC_{13-0} \leftarrow$ addr1 | | |
| | | PCDE | 2 | 3 | $PC_{13-0} \leftarrow PC_{13-8}$ + DE | | |
| | | PCXA | 2 | 3 | $PC_{13-0} \leftarrow PC_{13-8}$ + XA | | |
| | | BCDE | 2 | 3 | $PC_{13-0} \leftarrow$ BCDE[Note 2] | *6 | |
| | | BCXA | 2 | 3 | $PC_{13-0} \leftarrow$ BCXA[Note 2] | *6 | |
| | BRA[Note 1] | !addr1 | 3 | 3 | $PC_{13-0} \leftarrow$ addr1 | *11 | |
| | BRCB | !caddr | 2 | 2 | $PC_{13-0} \leftarrow PC_{13, 12}$ + $caddr_{11-0}$ | *8 | |

**Notes 1.** Double boxes indicate support for the Mk II mode only. Other areas indicate support for the Mk I mode only.

**2.** As for the B register, only the lower 2 bits are valid.

| Group | Mnemonic | Operand | No. of bytes | Machine cycle | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control | CALLA[Note] | !addr1 | 3 | 3 | $(SP - 6)(SP - 3)(SP - 4) \leftarrow PC_{11-0}$ <br> $(SP - 5) \leftarrow 0, 0, PC_{13,12}$ <br> $(SP - 2) \leftarrow X, X, MBE, RBE$ <br> $PC_{13-0} \leftarrow addr1, SP \leftarrow SP - 6$ | *11 | |
| | CALL[Note] | !addr | 3 | 3 | $(SP - 4)(SP - 1)(SP - 2) \leftarrow PC_{11-0}$ <br> $(SP - 3) \leftarrow MBE, RBE, PC_{13, 12}$ <br> $PC_{13-0} \leftarrow addr, SP \leftarrow SP - 4$ | *6 | |
| | | | | 4 | $(SP - 6)(SP - 3)(SP - 4) \leftarrow PC_{11-0}$ <br> $(SP - 5) \leftarrow 0, 0, PC_{13, 12}$ <br> $(SP - 2) \leftarrow X, X, MBE, RBE$ <br> $PC_{13-0} \leftarrow addr, SP \leftarrow SP - 6$ | | |
| | CALLF[Note] | !faddr | 2 | 2 | $(SP - 4)(SP - 1)(SP - 2) \leftarrow PC_{11-0}$ <br> $(SP - 3) \leftarrow MBE, RBE, PC_{13, 12}$ <br> $PC_{13-0} \leftarrow 000 + faddr, SP \leftarrow SP - 4$ | *9 | |
| | | | | 3 | $(SP - 6)(SP - 3)(SP - 4) \leftarrow PC_{11-0}$ <br> $(SP - 5) \leftarrow 0, 0, PC_{13, 12}$ <br> $(SP - 2) \leftarrow X, X, MBE, RBE$ <br> $PC_{13-0} \leftarrow 000 + faddr, SP \leftarrow SP - 6$ | | |
| | RET[Note] | | 1 | 3 | $MBE, RBE, PC_{13, 12} \leftarrow (SP + 1)$ <br> $PC_{11-0} \rightarrow (SP)(SP + 3)(SP + 2)$ <br> $SP \leftarrow SP + 4$ | | |
| | | | | | $X, X, MBE, RBE \leftarrow (SP + 4)$ <br> $PC_{11-0} \leftarrow (SP)(SP + 3)(SP + 2)$ <br> $0, 0, PC_{13, 12} \leftarrow (SP + 1)$ <br> $SP \leftarrow SP + 6$ | | |
| | RETS[Note] | | 1 | 3 + S | $MBE, RBE, PC_{13, 12} \leftarrow (SP + 1)$ <br> $PC_{11-0} \leftarrow (SP)(SP + 3)(SP + 2)$ <br> $SP \leftarrow SP + 4$ <br> then skip unconditionally | | Unconditional |
| | | | | | $X, X, MBE, RBE \leftarrow (SP + 4)$ <br> $PC_{11-0} \leftarrow (SP)(SP + 3)(SP + 2)$ <br> $0, 0, PC_{13, 12} \leftarrow (SP + 1)$ <br> $SP \leftarrow SP + 6$ <br> then skip unconditionally | | |
| | RETI | | 1 | 3 | $MBE, RBE, PC_{13, 12} \leftarrow (SP + 1)$ <br> $PC_{11-0} \leftarrow (SP)(SP + 3)(SP + 2)$ <br> $PSW \leftarrow (SP + 4)(SP + 5), SP \leftarrow SP + 6$ | | |
| | | | | | $0, 0, PC_{13, 12} \leftarrow SP + 1$ <br> $PC_{11-0} \leftarrow (SP)(SP + 3)(SP + 2)$ <br> $PSW \leftarrow (SP + 4)(SP + 5), SP \leftarrow SP + 6$ | | |

**Note**   Double boxes indicate support for the Mk II mode only.  Other areas indicate support for the Mk I mode only.

| Group | Mnemonic | Operand | No. of bytes | Machine cycle | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control | PUSH | rp | 1 | 1 | $(SP-1)(SP-2) \leftarrow rp$, $SP \leftarrow SP-2$ | | |
| | | BS | 2 | 2 | $(SP-1) \leftarrow MBS$, $(SP-2) \leftarrow RBS$, $SP \leftarrow SP-2$ | | |
| | POP | rp | 1 | 1 | $rp \leftarrow (SP+1)(SP)$, $SP \leftarrow SP+2$ | | |
| | | BS | 2 | 2 | $MBS \leftarrow (SP+1)$, $RBS \leftarrow (SP)$, $SP \leftarrow SP+2$ | | |
| Interrupt control | EI | | 2 | 2 | $IME(IPS.3) \leftarrow 1$ | | |
| | | IEXXX | 2 | 2 | $IEXXX \leftarrow 1$ | | |
| | DI | | 2 | 2 | $IME(IPS.3) \leftarrow 0$ | | |
| | | IEXXX | 2 | 2 | $IEXXX \leftarrow 0$ | | |
| I/O | IN[Note 1] | A, PORTn | 2 | 2 | $A \leftarrow PORTn$　　　(n = 0 to 6, 11) | | |
| | | XA, PORTn | 2 | 2 | $XA \leftarrow PORTn+1$, $PORTn$ (n = 4) | | |
| | OUT[Note 1] | PORTn, A | 2 | 2 | $PORTn \leftarrow A$　　　(n = 2 to 6) | | |
| | | PORTn, XA | 2 | 2 | $PORTn+1$, $PORTn \leftarrow XA$ (n = 4) | | |
| CPU control | HALT | | 2 | 2 | Set HALT Mode (PCC.2 $\leftarrow$ 1) | | |
| | STOP | | 2 | 2 | Set STOP Mode (PCC.3 $\leftarrow$ 1) | | |
| | NOP | | 1 | 1 | No Operation | | |
| Special | SEL | RBn | 2 | 2 | $RBS \leftarrow n$  (n = 0 to 3) | | |
| | | MBn | 2 | 2 | $MBS \leftarrow n$  (n = 0, 1, 15) | | |
| | GETI[Note 2, 3] | taddr | 1 | 3 | • When using TBR instruction<br>　$PC_{13\text{-}0} \leftarrow (taddr)_{5\text{-}0} + (taddr + 1)$ | *10 | |
| | | | | | • When using TCALL instruction<br>　$(SP-4)(SP-1)(SP-2) \leftarrow PC_{11\text{-}0}$<br>　$(SP-3) \leftarrow MBE, RBE, PC_{13, 12}$<br>　$PC_{13\text{-}0} \leftarrow (taddr)_{5\text{-}0} + (taddr + 1)$<br>　$SP \leftarrow SP-4$ | | |
| | | | | | • When using instruction other than TBR or TCALL<br>Execute (taddr)(taddr + 1) instructions | | Determined by referenced instruction |
| | | | 1 | 3 | • When using TBR instruction<br>　$PC_{13\text{-}0} \leftarrow (taddr)_{5\text{-}0} + (taddr + 1)$ | *10 | |
| | | | | 4 | • When using TCALL instruction<br>　$(SP-6)(SP-3)(SP-4) \leftarrow PC_{11\text{-}0}$<br>　$(SP-5) \leftarrow 0, 0, PC_{13, 12}$<br>　$(SP-2) \leftarrow X, X, MBE, RBE$<br>　$PC_{13\text{-}0} \leftarrow (taddr)_{5\text{-}0} + (taddr + 1)$<br>　$SP \leftarrow SP-6$ | | |
| | | | | 3 | • When using instruction other than TBR or TCALL<br>Execute (taddr)(taddr + 1) instructions | | Determined by referenced instruction |

**Notes 1.** Before executing the IN or OUT instruction, set MBE to  0 or 1 and set MBS to 15.

**2.** TBR and TCALL instructions are assembler pseudo-instructions for the GETI instruction's table definitions.

**3.** Double box indicates support for the Mk II mode only.  Other areas indicate support for the Mk I mode only.

## 8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The program memory in the $\mu$PD75P0076 is a 16384 x 8-bit electronic write-enabled one-time PROM. The pins listed in the table below are used for this PROM's write/verify operations. Clock input from the X1 pins is used instead of address input as a method for updating addresses.

| Pin name | Function |
|---|---|
| VPP | Pin (usually VDD) where programming voltage is applied during program memory write/verify |
| X1, X2 | Clock input pin for address updating during program memory write/verify. Input the X1 pin's inverted signal to the X2 pin. |
| MD0 to MD3 | Operation mode selection pin for program memory write/verify |
| D0/P40 to D3/P43 (lower 4) D4/P50 to D7/P53 (upper 4) | 8-bit data I/O pin for program memory write/verify |
| VDD | Pin where power supply voltage is applied. Power voltage range for normal operation is 1.8 to 5.5 V. Apply 6 V for program memory write/verify. |

**Caution  Pins not used for program memory write/verify should be handled as follows.**
   **• All unused pins except XT2 ...... Connect to Vss via a pull-down resistor**
   **• XT2 pin ........................................ Leave open**

### 8.1 Operation Modes for Program Memory Write/Verify

When +6 V is applied to the $\mu$PD75P0076's VDD pin and +12.5 V is applied to its VPP pin, program memory write/verify modes are in effect. Furthermore, the following detailed operation modes can be specified by setting pins MD0 to MD3 as shown below.

| Operation mode specification | | | | | | Operation mode |
|---|---|---|---|---|---|---|
| VPP | VDD | MD0 | MD1 | MD2 | MD3 | |
| +12.5 V | +6 V | H | L | H | L | Zero-clear program memory address |
| | | L | H | H | H | Write mode |
| | | L | L | H | H | Verify mode |
| | | H | X | H | H | Program inhibit mode |

X: L or H

### 8.2  Steps in Program Memory Write Operation

High-speed program memory write can be executed via the following steps.

(1)  Pull down unused pins to Vss via resistors.  Set the X1 pin to low.

(2)  Apply +5 V to the VDD and VPP pins.

(3)  Wait 10 $\mu$s.

(4)  Zero-clear mode for program memory addresses.

(5)  Apply +6 V to VDD and +12.5 V to VPP.

(6)  Write data using 1-ms write mode.

(7)  Verify mode.  If write is verified, go to step (8) and if write is not verified, go back to steps (6) to (7).

(8)  X [= number of write operations from steps (6) to (7)] x 1 ms additional write

(9)  4 pulse inputs to the X1 pin updates (increments +1) the program memory address.

(10) Repeat steps (6) to (9) until the last address is completed.

(11) Zero-clear mode for program memory addresses.

(12) Apply +5 V to the VDD and VPP pins.

(13) Power supply OFF

The following diagram illustrates steps (2) to (9).
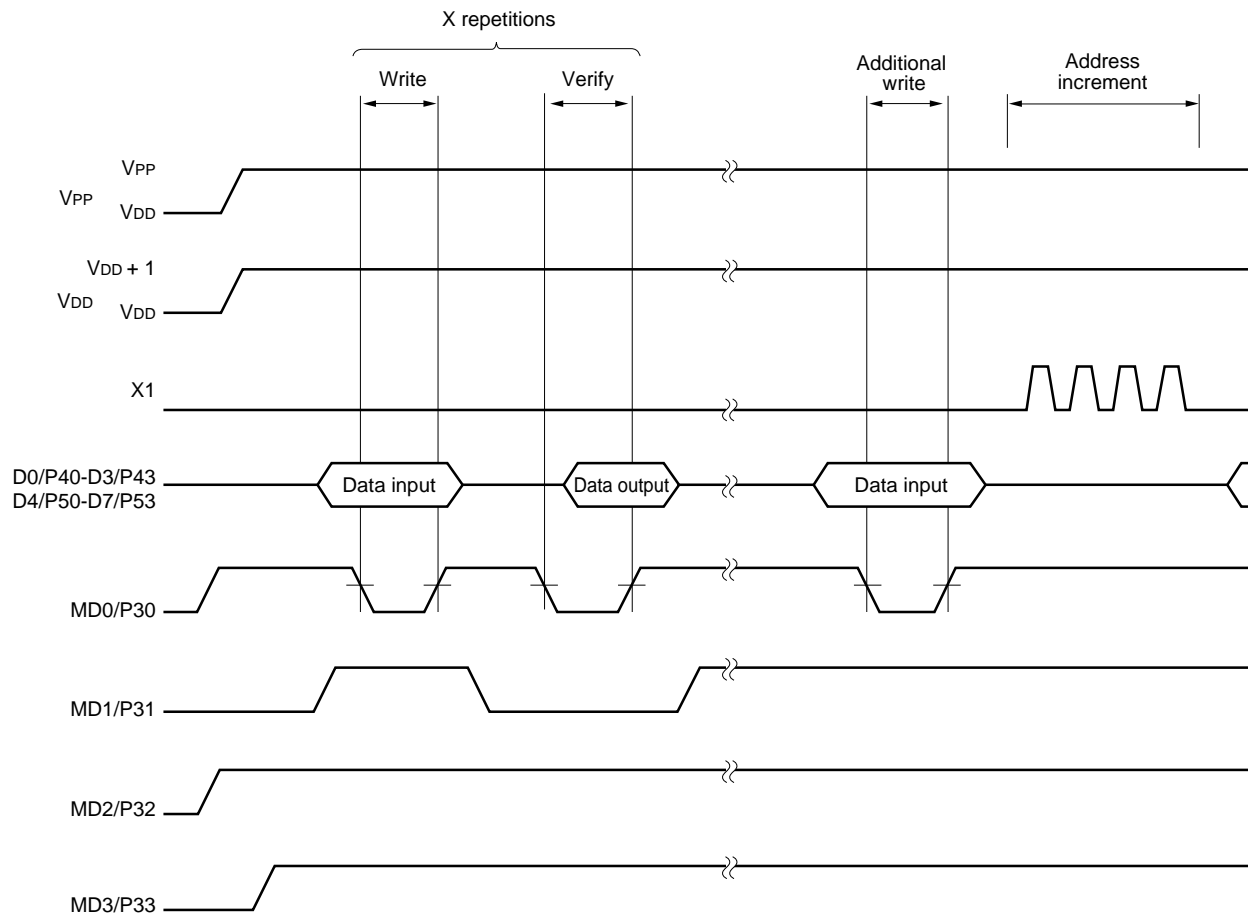
### 8.3 Steps in Program Memory Read Operation

The $\mu$PD75P0076 can read out the program memory contents via the following steps.

(1)   Pull down unused pins to V$_{SS}$ via resistors.  Set the X1 pin to low.

(2)   Apply +5 V to the V$_{DD}$ and V$_{PP}$ pins.

(3)   Wait 10 $\mu$s.

(4)   Zero-clear mode for program memory addresses.

(5)   Apply +6 V to V$_{DD}$ and +12.5 V to V$_{PP}$.

(6)   Verify mode.  When a clock pulse is input to the X1 pin, data is output sequentially to one address at a time based on a cycle of four pulse inputs.

(7)   Zero-clear mode for program memory addresses.

(8)   Apply +5 V to the V$_{DD}$ and V$_{PP}$ pins.

(9)   Power supply OFF

The following diagram illustrates steps (2) to (7).
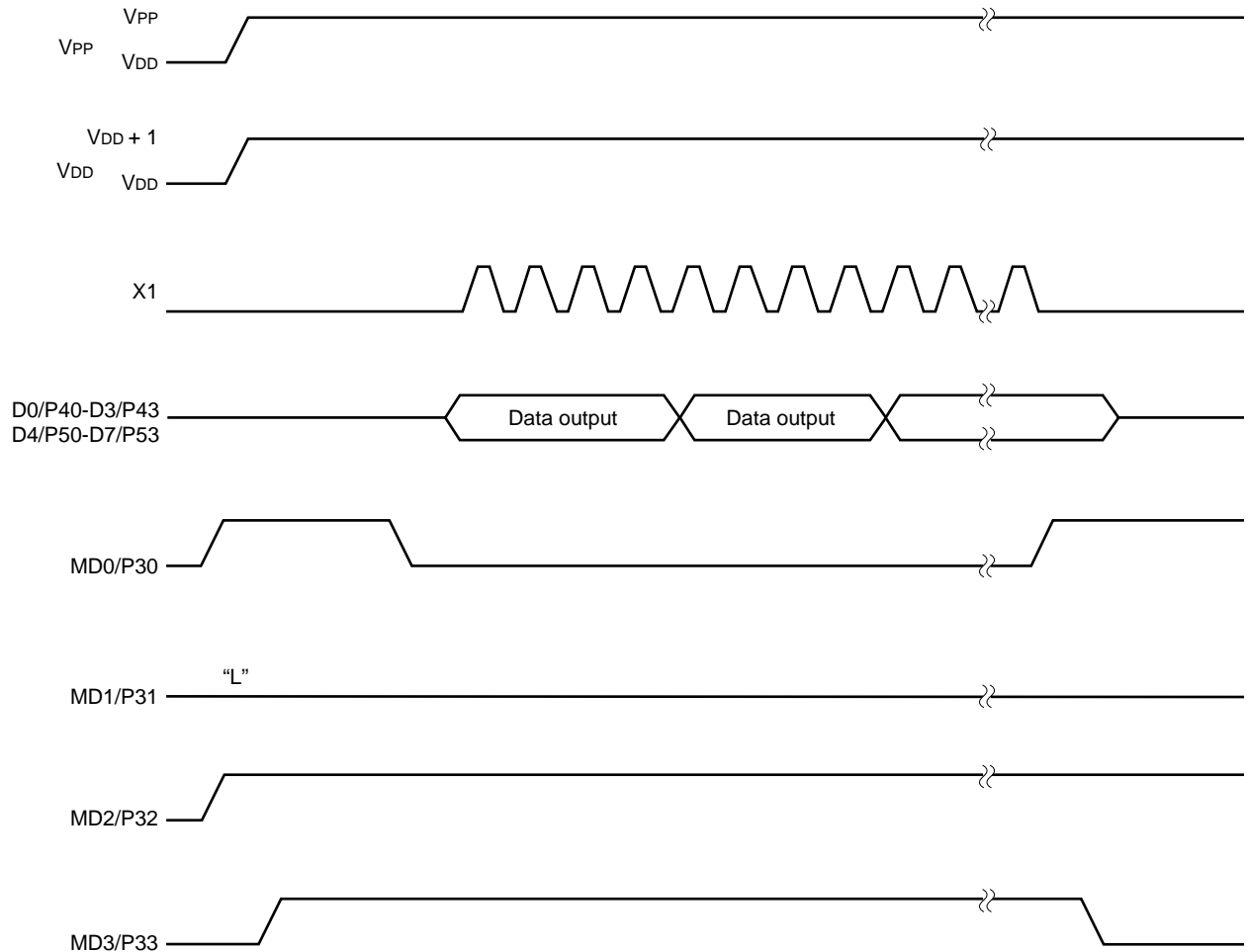
**8.4  One-Time PROM Screening**

Due to its structure, the one-time PROM cannot be fully tested before shipment by NEC.  Therefore, NEC recommends the screening process, that is, after the required data is written to the PROM and the PROM is stored under the high-temperature conditions shown below, the PROM should be verified.

| Storage temperature | Storage time |
|---|---|
| 125 ˚C | 24 hours |

★ **9. ELECTRICAL SPECIFICATIONS**
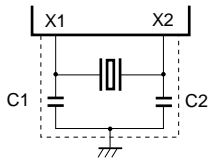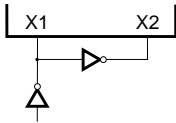
**ABSOLUTE MAXIMUM RATINGS (T$_A$ = 25˚C)**
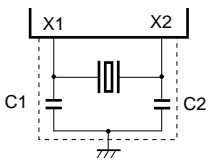
| Parameter | Symbol | Test Conditions | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | V$_{DD}$ | | −0.3 to +7.0 | V |
| PROM power supply voltage | V$_{PP}$ | | −0.3 to +13.5 | V |
| Input voltage | V$_{I1}$ | Except ports 4, 5 | −0.3 to V$_{DD}$ +0.3 | V |
| | V$_{I2}$ | Ports 4, 5 (N-ch open drain) | −0.3 to +14 | V |
| Output voltage | V$_O$ | | −0.3 to V$_{DD}$ +0.3 | V |
| Output current high | I$_{OH}$ | Per pin | −10 | mA |
| | | Total of all pins | −30 | mA |
| Output current low | I$_{OL}$ | Per pin | 30 | mA |
| | | Total of all pins | 220 | mA |
| Operating ambient temperature | T$_A$ | | −40 to +85 | ˚C |
| Storage temperature | T$_{stg}$ | | −65 to +150 | ˚C |

**Caution   If any of the parameters exceeds the absolute maximum ratings, even momentarily, the reliability of the product may be impaired.  The absolute maximum ratings are values that may physically damage the products.  Be sure to use the products within the ratings.**

**CAPACITANCE (T$_A$ = 25˚C, V$_{DD}$ = 0 V)**

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | C$_{IN}$ | f = 1 MHz Unmeasured pins returned to 0 V. | | | 15 | pF |
| Output capacitance | C$_{OUT}$ | | | | 15 | pF |
| I/O capacitance | C$_{IO}$ | | | | 15 | pF |

**MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)**
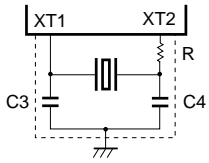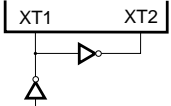
| Resonator | Recommended constant | Parameter | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Ceramic resonator | X1 X2 C1 C2 | Oscillation frequency (fx)[Note 1] | | 1.0 | | 6.0[Note 2] | MHz |
| | | Oscillation stabilization time[Note 3] | After V$_{DD}$ reaches oscillation voltage range MIN. | | | 4 | ms |
| Crystal resonator | X1 X2 C1 C2 | Oscillation frequency (fx)[Note 1] | | 1.0 | | 6.0[Note 2] | MHz |
| | | Oscillation stabilization time[Note 3] | V$_{DD}$ = 4.5 to 5.5 V | | | 10 | ms |
| | | | | | | 30 | |
| External clock | X1 X2 | X1 input frequency (fx)[Note 1] | | 1.0 | | 6.0[Note 2] | MHz |
| | | X1 input high-/low-level width (t$_{XH}$, t$_{XL}$) | | 83.3 | | 500 | ns |

**Notes 1.** The oscillation frequency and X1 input frequency indicate characteristics of the oscillator only. For the instruction execution time, refer to AC Characteristics.

**2.** When the power supply voltage is 1.8 V ≤ V$_{DD}$ < 2.7 V and the oscillation frequency is 4.19 MHz < fx ≤ 6.0 MHz, setting the processor clock control register (PCC) to 0011 results in 1 machine cycle being less than the required 0.95 $\mu$s. Therefore, set PCC to a value other than 0011.

**3.** The oscillation stabilization time is necessary for oscillation to stabilize after applying V$_{DD}$ or releasing the STOP mode.

**Caution** **When using the main system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V$_{SS}$.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

**SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T$_A$ = −40 to +85˚C, V$_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended constant | Parameter | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Crystal resonator | XT1 XT2 R C3 C4 | Oscillation frequency (f$_{XT}$)[Note 1] | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization time[Note 2] | V$_{DD}$ = 4.5 to 5.5 V | | 1.0 | 2 | s |
| | | | | | | 10 | |
| External clock | XT1 XT2 | XT1 input frequency (f$_{XT}$)[Note 1] | | 32 | | 100 | kHz |
| | | XT1 input high-/low-level width (t$_{XTH}$, t$_{XTL}$) | | 5 | | 15 | $\mu$s |

**Notes 1.** Indicates only oscillator characteristics.  Refer to AC Characteristics for instruction execution time.
    **2.** The oscillation stabilization time is necessary for oscillation to stabilize after applying V$_{DD}$.

**Caution   When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V$_{SS}$.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

**The subsystem clock oscillator is designed as a low amplification circuit to provide low consumption current, causing misoperation by noise more frequently than the main system clock oscillation circuit.  Special care should therefore be taken for wiring method when the subsystem clock is used.**

**RECOMMENDED OSCILLATION CIRCUIT CONSTANTS**

**CERAMIC RESONATOR (T$_A$ = –20 to +80 ˚C)**

| Manufacturer | Product Name | Frequency (MHz) | Oscillation Circuit Constants (pF) | | Oscillation Voltage Range (V$_{DD}$) | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2 | MIN. | MAX. | |
| Murata Mfg. Co., Ltd. | CSB1000J**Note** | 1.0 | 100 | 100 | 2.2 | 5.5 | Rd = 5.6 K$\Omega$ |
| | CSA2.00MG040 | 2.0 | 100 | 100 | 2.0 | | — |
| | CST2.00MG040 | | — | — | | | With on-chip capacitor |
| | CSA4.00MG | 4.0 | 30 | 30 | 1.8 | | — |
| | CST4.00MGW | | — | — | | | With on-chip capacitor |
| | CSA4.19MG | 4.19 | 30 | 30 | | | — |
| | CST4.19MGW | | — | — | | | With on-chip capacitor |
| | CSA6.00MG | 6.0 | 30 | 30 | 2.6 | | — |
| | CST6.00MGW | | — | — | | | With on-chip capacitor |
| | CSA6.00MGU | | 30 | 30 | 1.8 | | — |
| | CST6.00MGWU | | — | — | | | With on-chip capacitor |

**Note**  When the CSB1000J (1.0 MHz) manufactured by Murata Mfg. is used as a ceramic resonator, a limiting resistor (Rd = 5.6 k$\Omega$) is required (see the figure below).  Other recommended resonators do not require such a limiting resistor.
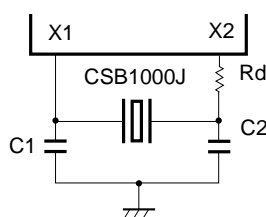


**Caution**   **The oscillation circuit constants and oscillation voltage range only indicate the conditions under which the circuit can oscillate stably, and do not guarantee the oscillation frequency accuracy.  If oscillation frequency accuracy is required in the actual circuit, it is necessary to adjust oscillation frequencies in the actual circuit, and you should consult directly with the manufacturer of the resonator used.**

**DC CHARACTERISTICS (T$_A$ = −40 to +85˚C, V$_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Output current low | I$_{OL}$ | Per pin | | | | | 15 | mA |
| | | Total of all pins | | | | | 150 | mA |
| Input voltage high | V$_{IH1}$ | Ports 2, 3, and 11 | 2.7 ≤ V$_{DD}$ ≤ 5.5 V | | 0.7V$_{DD}$ | | V$_{DD}$ | V |
| | | | 1.8 ≤ V$_{DD}$ < 2.7 V | | 0.9V$_{DD}$ | | V$_{DD}$ | V |
| | V$_{IH2}$ | Ports 0, 1, 6, $\overline{RESET}$ | 2.7 ≤ V$_{DD}$ ≤ 5.5 V | | 0.8V$_{DD}$ | | V$_{DD}$ | V |
| | | | 1.8 ≤ V$_{DD}$ < 2.7 V | | 0.9V$_{DD}$ | | V$_{DD}$ | V |
| | V$_{IH3}$ | Ports 4, 5 | 2.7 ≤ V$_{DD}$ ≤ 5.5 V | | 0.7V$_{DD}$ | | 13 | V |
| | | (N-ch open-drain) | 1.8 ≤ V$_{DD}$ < 2.7 V | | 0.9V$_{DD}$ | | 13 | V |
| | V$_{IH4}$ | X1, XT1 | | | V$_{DD}$ − 0.1 | | V$_{DD}$ | V |
| Input voltage low | V$_{IL1}$ | Ports 2-5, 11 | 2.7 ≤ V$_{DD}$ ≤ 5.5 V | | 0 | | 0.3V$_{DD}$ | V |
| | | | 1.8 ≤ V$_{DD}$ < 2.7 V | | 0 | | 0.1V$_{DD}$ | V |
| | V$_{IL2}$ | Ports 0, 1, 6, $\overline{RESET}$ | 2.7 ≤ V$_{DD}$ ≤ 5.5 V | | 0 | | 0.2V$_{DD}$ | V |
| | | | 1.8 ≤ V$_{DD}$ < 2.7 V | | 0 | | 0.1V$_{DD}$ | V |
| | V$_{IL3}$ | X1, XT1 | | | 0 | | 0.1 | V |
| Output voltage high | V$_{OH}$ | $\overline{SCK}$, SO, Ports 2, 3, 6   I$_{OH}$ = −1.0 mA | | | V$_{DD}$ − 0.5 | | | V |
| Output voltage low | V$_{OL1}$ | $\overline{SCK}$, SO, Ports 2-6 | I$_{OL}$ = 15 mA, V$_{DD}$ = 4.5 to 5.5 V | | | 0.2 | 2.0 | V |
| | | | I$_{OL}$ = 1.6 mA | | | | 0.4 | V |
| | V$_{OL2}$ | SB0, SB1 | When N-ch open-drain pull-up resistor ≥ 1 kΩ | | | | 0.2V$_{DD}$ | V |
| Input leakage current high | I$_{LIH1}$ | V$_{IN}$ = V$_{DD}$ | Pins other than X1, XT1 | | | | 3 | $\mu$A |
| | I$_{LIH2}$ | | X1, XT1 | | | | 20 | $\mu$A |
| | I$_{LIH3}$ | V$_{IN}$ = 13 V | Ports 4, 5 (N-ch open-drain) | | | | 20 | $\mu$A |
| Input leakage current low | I$_{LIL1}$ | V$_{IN}$ = 0 V | Ports 4, 5, pins other than X1, XT1 | | | | −3 | $\mu$A |
| | I$_{LIL2}$ | | X1, XT1 | | | | −20 | $\mu$A |
| | I$_{LIL3}$ | | Ports 4, 5 (N-ch open-drain) When input instruction is not executed | | | | −3 | $\mu$A |
| | | | Ports 4, 5 (N-ch open-drain)  When input instruction is executed | | | | −30 | $\mu$A |
| | | | | V$_{DD}$ = 5.0 V | | −10 | −27 | $\mu$A |
| | | | | V$_{DD}$ = 3.0 V | | −3 | −8 | $\mu$A |
| Output leakage current high | I$_{LOH1}$ | V$_{OUT}$ = V$_{DD}$ | $\overline{SCK}$, SO/SB0, SB1, Ports 2, 3, 6 | | | | 3 | $\mu$A |
| | I$_{LOH2}$ | V$_{OUT}$ = 13 V | Ports 4, 5 (N-ch open-drain) | | | | 20 | $\mu$A |
| Output leakage current low | I$_{LOL}$ | V$_{OUT}$ = 0 V | | | | | −3 | $\mu$A |
| On-chip pull-up resistor | R$_L$ | V$_{IN}$ = 0 V | Ports 0-3, 6 (Excluding P00 pin) | | 50 | 100 | 200 | kΩ |

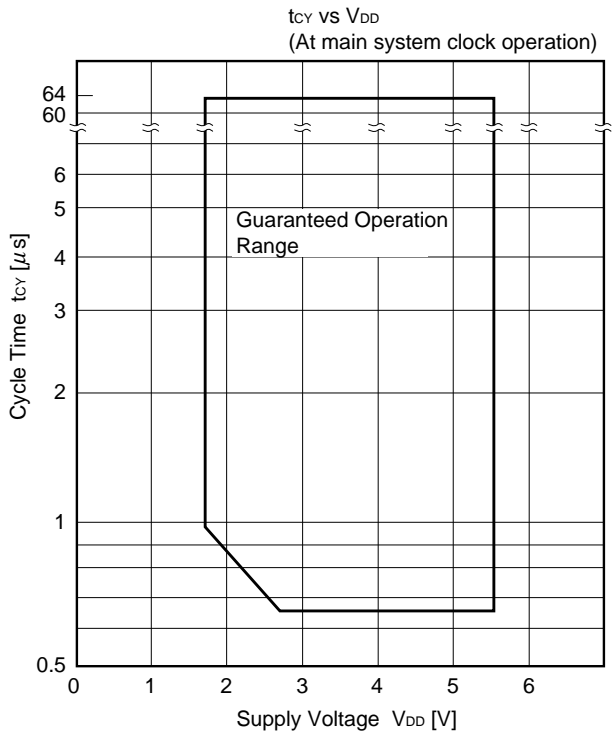**DC CHARACTERISTICS (T$_A$ = −40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | I$_{DD1}$ | 6.0 MHz Note 2 | V$_{DD}$ = 5.0 V ± 10% Note 3 | | | 3.4 | 10.2 | mA |
| | | Crystal oscillation | V$_{DD}$ = 3.0 V ± 10% Note 4 | | | 0.8 | 2.4 | mA |
| | I$_{DD2}$ | C1 = C2 = 22 pF | HALT mode | V$_{DD}$ = 5.0 V ± 10% | | 0.9 | 2.7 | mA |
| | | | | V$_{DD}$ = 3.0 V ± 10% | | 0.5 | 1.5 | mA |
| | I$_{DD1}$ | 4.19 MHz Note 2 | V$_{DD}$ = 5.0 V ± 10% Note 3 | | | 2.7 | 7.4 | mA |
| | | Crystal oscillation | V$_{DD}$ = 3.0 V ± 10% Note 4 | | | 0.6 | 1.8 | mA |
| | I$_{DD2}$ | C1 = C2 = 22 pF | HALT mode | V$_{DD}$ = 5.0 V ± 10% | | 0.8 | 2.4 | mA |
| | | | | V$_{DD}$ = 3.0 V ± 10% | | 0.4 | 1.2 | mA |
| | I$_{DD3}$ | 32.768 kHz Note 5 | Low-voltage mode Note 6 | V$_{DD}$ = 3.0 V ± 10% | | 42 | 126 | μA |
| | | Crystal oscillation | | V$_{DD}$ = 2.0 V ± 10% | | 23 | 69 | μA |
| | | | | V$_{DD}$ = 3.0 V, T$_A$ = 25°C | | 42 | 84 | μA |
| | | | Low current consumption mode Note 7 | V$_{DD}$ = 3.0 V ± 10% | | 40 | 120 | μA |
| | | | | V$_{DD}$ = 3.0 V, T$_A$ = 25°C | | 40 | 80 | μA |
| | I$_{DD4}$ | | HALT mode | Low-voltage mode Note 6 — V$_{DD}$ = 3.0 V ± 10% | | 8 | 24 | μA |
| | | | | V$_{DD}$ = 2.0 V ± 10% | | 4 | 12 | μA |
| | | | | V$_{DD}$ = 3.0 V, T$_A$ = 25°C | | 8 | 16 | μA |
| | | | | Low current consumption mode Note 7 — V$_{DD}$ = 3.0 V ± 10% | | 7 | 21 | μA |
| | | | | V$_{DD}$ = 3.0 V, T$_A$ = 25°C | | 7 | 14 | μA |
| | I$_{DD5}$ | XT1 = 0 V | V$_{DD}$ = 5.0 V ± 10% | | | 0.05 | 10 | μA |
| | | STOP mode Note 8 | V$_{DD}$ = 3.0 V | | | 0.02 | 5.0 | μA |
| | | ± 10% | T$_A$ = 25°C | | | 0.02 | 3.0 | μA |

**Notes 1.** Not including currents flowing in on-chip pull-up resistors.

**2.** Including oscillation of the subsystem clock.

**3.** When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

**4.** When PCC is set to 0000 and the device is operated in the low-speed mode.

**5.** When the system clock control register (SCC) is set to 1001 and the device is operated on the subsystem clock, with main system clock oscillation stopped.

**6.** When the sub-oscillation circuit control register (SOS) is set to 0000.

**7.** When SOS is set to 0010.

**8.** When SOS is set to 00×1, the feedback resistors of the sub-oscillation circuit is cutoff. (×: don't care)

**AC CHARACTERISTICS (T<sub>A</sub> = –40 to +85˚C, V<sub>DD</sub> = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| CPU clock cycle time [Note 1] (Minimum instruction execution time = 1 machine cycle) | $t_{CY}$ | Operating on main system clock | $V_{DD}$ = 2.7 to 5.5 V | 0.67 | | 64 | $\mu$s |
| | | | | 0.95 | | 64 | $\mu$s |
| | | Operating on subsystem clock | | 114 | 122 | 125 | $\mu$s |
| TI0, TI1 input frequency | $f_{TI}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0 | | 1.0 | MHz |
| | | | | 0 | | 275 | kHz |
| TI0, TI1 input high-/low-level width | $t_{TIH}$, $t_{TIL}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0.48 | | | $\mu$s |
| | | | | 1.8 | | | $\mu$s |
| Interrupt input high-/low-level width | $t_{INTH}$, $t_{INTL}$ | INT0 | IM02 = 0 | **Note 2** | | | $\mu$s |
| | | | IM02 = 1 | 10 | | | $\mu$s |
| | | INT1, 2, 4 | | 10 | | | $\mu$s |
| | | KR0 to KR3 | | 10 | | | $\mu$s |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | $\mu$s |

**Notes 1.** The cycle time (minimum instruction execution time) of the CPU clock ($\Phi$) is determined by the oscillation frequency of the connected resonator (and external clock), the system clock control register (SCC) and the processor clock control register (PCC). The figure at the right indicates the cycle time $t_{CY}$ versus supply voltage $V_{DD}$ characteristic with the main system clock operating.

**2.** $2t_{CY}$ or $128/f_x$ is set by setting the interrupt mode register (IM0).



$t_{CY}$ vs $V_{DD}$
(At main system clock operation)

**SERIAL TRANSFER OPERATION**

**2-Wire and 3-Wire Serial I/O Mode ($\overline{SCK}$...Internal clock output): (T$_A$ = −40 to +85˚C, V$_{DD}$ = 1.8 to 5.5 V)**

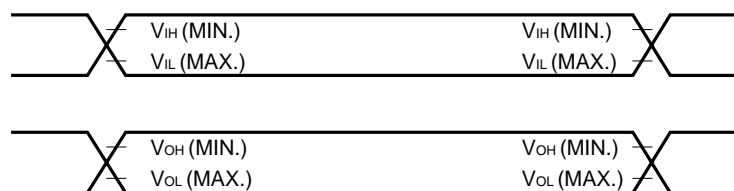| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | t$_{KCY1}$ | V$_{DD}$ = 2.7 to 5.5 V | | 1300 | | | ns |
| | | | | 3800 | | | ns |
| $\overline{SCK}$ high-/low-level width | t$_{KL1}$, t$_{KH1}$ | V$_{DD}$ = 2.7 to 5.5 V | | t$_{KCY1}$/2−50 | | | ns |
| | | | | t$_{KCY1}$/2−150 | | | ns |
| SI[Note 1] setup time (to $\overline{SCK}$↑) | t$_{SIK1}$ | V$_{DD}$ = 2.7 to 5.5 V | | 150 | | | ns |
| | | | | 500 | | | ns |
| SI[Note 1] hold time (from $\overline{SCK}$↑) | t$_{KSI1}$ | V$_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 600 | | | ns |
| $\overline{SCK}$↓→SO[Note 1] output delay time | t$_{KSO1}$ | R$_L$ = 1 kΩ, C$_L$ = 100 pF[Note 2] | V$_{DD}$ = 2.7 to 5.5 V | 0 | | 250 | ns |
| | | | | 0 | | 1000 | ns |

Notes 1. In 2-wire serial I/O mode, read SB0 or SB1 instead.
2. R$_L$ and C$_L$ are the load resistance and load capacitance of the SO output lines.

**2-Wire and 3-Wire Serial I/O Mode ($\overline{SCK}$...External clock input): (T$_A$ = −40 to +85˚C, V$_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | t$_{KCY2}$ | V$_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | | | 3200 | | | ns |
| $\overline{SCK}$ high-/low-level width | t$_{KL2}$, t$_{KH2}$ | V$_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 1600 | | | ns |
| SI[Note 1] setup time (to $\overline{SCK}$↑) | t$_{SIK2}$ | V$_{DD}$ = 2.7 to 5.5 V | | 100 | | | ns |
| | | | | 150 | | | ns |
| SI[Note 1] hold time (from $\overline{SCK}$↑) | t$_{KSI2}$ | V$_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 600 | | | ns |
| $\overline{SCK}$↓→SO[Note 1] output delay time | t$_{KSO2}$ | R$_L$ = 1 kΩ, C$_L$ = 100 pF[Note 2] | V$_{DD}$ = 2.7 to 5.5 V | 0 | | 300 | ns |
| | | | | 0 | | 1000 | ns |

Notes 1. In 2-wire serial I/O mode, read SB0 or SB1 instead.
2. R$_L$ and C$_L$ are the load resistance and load capacitance of the SO output lines.

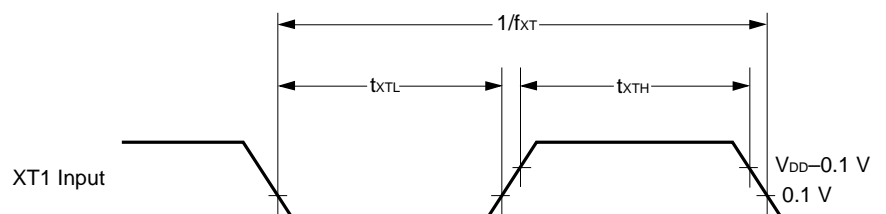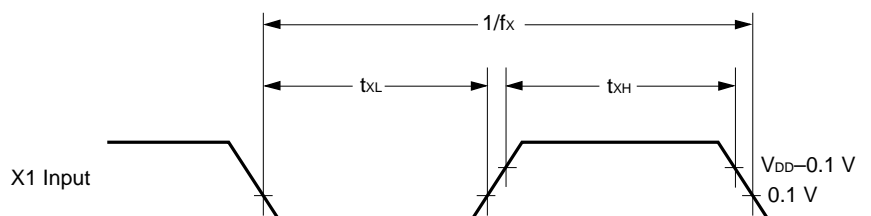**A/D CONVERTER CHARACTERISTICS ($T_A$ = −40 to +85 ˚C, $V_{DD}$ = 1.8 to 5.5 V, 1.8 V $\leq$ AV$_{REF}$ $\leq$ V$_{DD}$)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | | | | 8 | 8 | 8 | bit |
| Absolute accuracy[Note 1] | | $V_{DD}$ = AV$_{REF}$ | 2.7 $\leq$ V$_{DD}$ | | | 1.5 | LSB |
| | | | 1.8 V $\leq$ V$_{DD}$ < 2.7 V | | | 3 | LSB |
| | | $V_{DD}$ $\neq$ AV$_{REF}$ | | | | 3 | LSB |
| Conversion time[Note 2] | $t_{CONV}$ | | | | | 168/$f_X$ | $\mu$s |
| Sampling time[Note 3] | $t_{SAMP}$ | | | | | 44/$f_X$ | $\mu$s |
| Analog input voltage | $V_{IAN}$ | | | AV$_{SS}$ | | AV$_{REF}$ | V |
| Analog input impedance | $R_{AN}$ | | | | 1000 | | M$\Omega$ |
| AV$_{REF}$ current | $I_{REF}$ | | | | 0.25 | 2.0 | mA |

**Notes 1.** Absolute accuracy excluding quantization error ($\pm$1/2 LSB).

**2.** Time after execution of conversion start instruction until completion of conversion (EOC = 1) (40.1 $\mu$s: in $f_X$ = 4.19 MHz operation)

**3.** Time after conversion start instruction until completion of sampling (10.5 $\mu$s: in $f_X$ = 4.19 MHz operation)
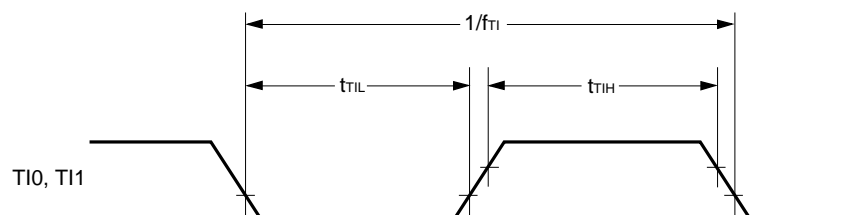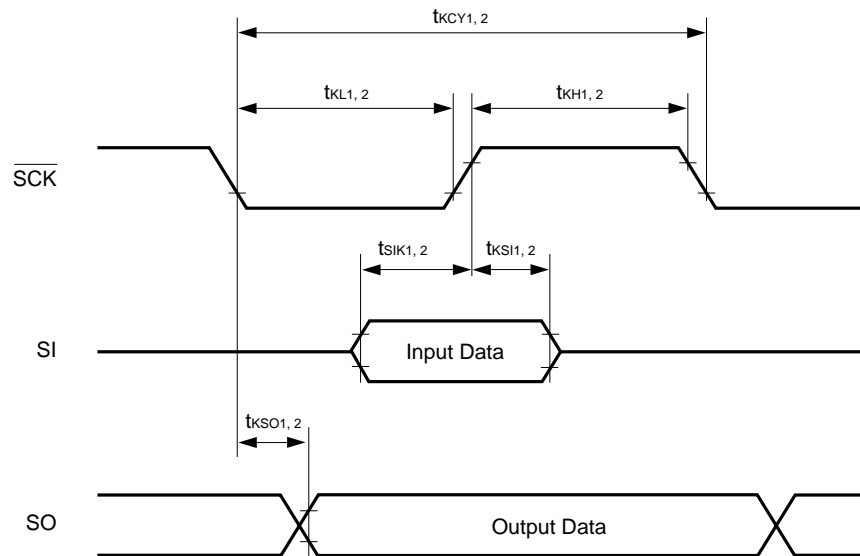
**AC Timing Test Point (Excluding X1, XT1 Input)**

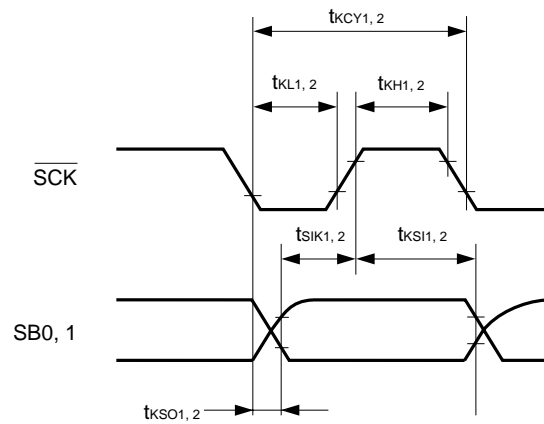| | V_IH (MIN.) | V_IH (MIN.) | |
|---|---|---|---|
| | V_IL (MAX.) | V_IL (MAX.) | |

$V_{IH}$ (MIN.)  $V_{IH}$ (MIN.)
$V_{IL}$ (MAX.)  $V_{IL}$ (MAX.)

$V_{OH}$ (MIN.)  $V_{OH}$ (MIN.)
$V_{OL}$ (MAX.)  $V_{OL}$ (MAX.)

**Clock Timing**

$1/f_X$, $t_{XL}$, $t_{XH}$

X1 Input — $V_{DD}$–0.1 V, 0.1 V

$1/f_{XT}$, $t_{XTL}$, $t_{XTH}$

XT1 Input — $V_{DD}$–0.1 V, 0.1 V

**TI0, TI1 Timing**

$1/f_{TI}$, $t_{TIL}$, $t_{TIH}$

TI0, TI1

**Serial Transfer Timing**

**3-wire serial I/O mode**



**2-wire serial I/O mode**

**Interrupt input timing**

INT0, 1, 2, 4
KR0 to 3

$t_{INTL}$ $t_{INTH}$
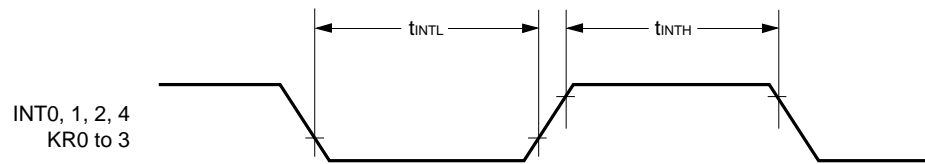
$\overline{\text{RESET}}$ **input timing**

$\overline{\text{RESET}}$

$t_{RSL}$
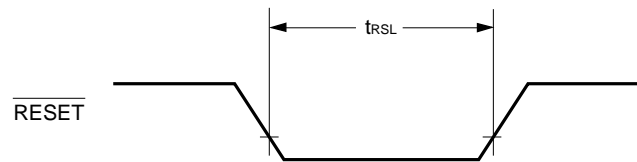
**DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS**

**($T_A$ = −40 to +85˚C)**

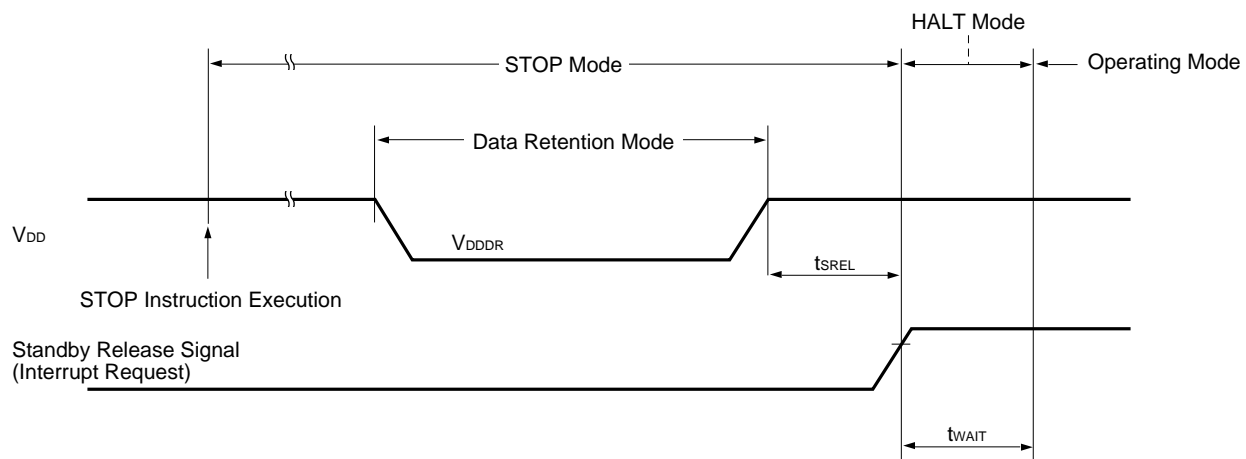| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Release signal set time | $t_{SREL}$ | | 0 | | | $\mu$s |
| Oscillation stabilization wait time[Note 1] | $t_{WAIT}$ | Release by $\overline{\text{RESET}}$ | | $2^{15}/f_x$ | | ms |
| | | Release by interrupt request | | **Note 2** | | ms |

**Notes 1.** The oscillation stabilization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the oscillation start.

**2.** Depends on the basic interval timer mode register (BTM) settings (See the table below).

| BTM3 | BTM2 | BTM1 | BTM0 | Wait time | |
|---|---|---|---|---|---|
| | | | | $f_x$ = at 4.19 MHz | $f_x$ = at 6.0 MHz |
| — | 0 | 0 | 0 | $2^{20}/f_x$ (approx. 250 ms) | $2^{20}/f_x$ (approx. 175 ms) |
| — | 0 | 1 | 1 | $2^{17}/f_x$ (approx. 31.3 ms) | $2^{17}/f_x$ (approx. 21.8 ms) |
| — | 1 | 0 | 1 | $2^{15}/f_x$ (approx. 7.81 ms) | $2^{15}/f_x$ (approx. 5.46 ms) |
| — | 1 | 1 | 1 | $2^{13}/f_x$ (approx. 1.95 ms) | $2^{13}/f_x$ (approx. 1.37 ms) |

**Data Retention Timing (STOP Mode Release by RESET)**

Internal Reset Operation

HALT Mode

STOP Mode —— Operating Mode

Data Retention Mode

$V_{DD}$

$V_{DDDR}$

$t_{SREL}$

STOP Instruction Execution

$\overline{\text{RESET}}$

$t_{WAIT}$
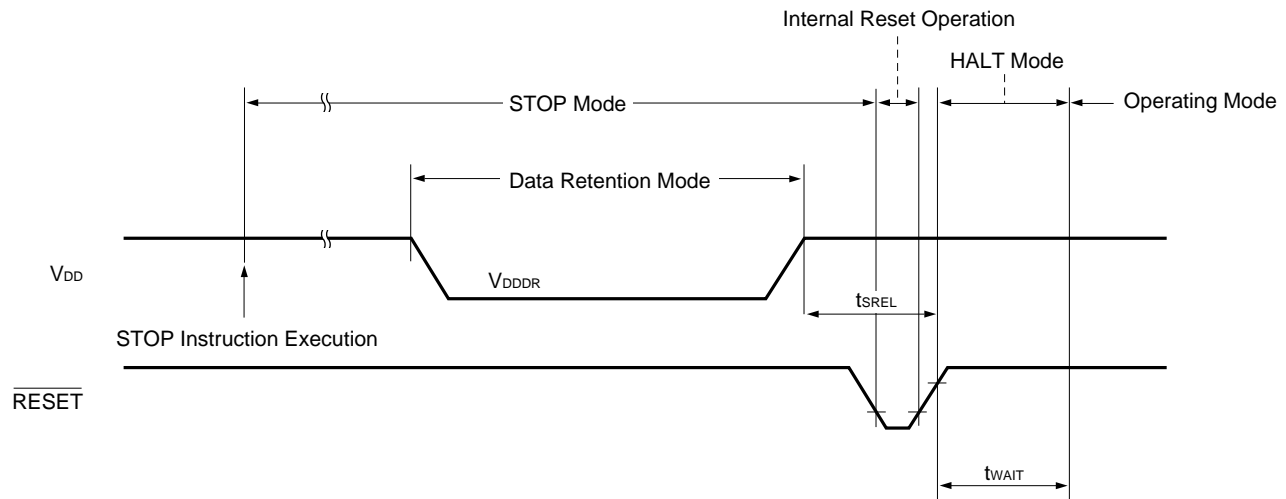
**Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)**

HALT Mode

STOP Mode —— Operating Mode

Data Retention Mode

$V_{DD}$

$V_{DDDR}$

$t_{SREL}$

STOP Instruction Execution

Standby Release Signal
(Interrupt Request)

$t_{WAIT}$

**DC PROGRAMMING CHARACTERISTICS (T$_A$ = 25 $\pm$ 5˚C, V$_{DD}$ = 6.0 $\pm$ 0.25 V, V$_{PP}$ = 12.5 $\pm$ 0.3 V, V$_{SS}$ = 0 V)**

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input voltage high | V$_{IH1}$ | Except X1, X2 | 0.7V$_{DD}$ | | V$_{DD}$ | V |
| | V$_{IH2}$ | X1, X2 | V$_{DD}$−0.5 | | V$_{DD}$ | V |
| Input voltage low | V$_{IL1}$ | Except X1, X2 | 0 | | 0.3V$_{DD}$ | V |
| | V$_{IL2}$ | X1, X2 | 0 | | 0.4 | V |
| Input leakage current | I$_{LI}$ | V$_{IN}$ = V$_{IL}$ or V$_{IH}$ | | | 10 | $\mu$A |
| Output voltage high | V$_{OH}$ | I$_{OH}$ = −1 mA | V$_{DD}$−1.0 | | | V |
| Output voltage low | V$_{OL}$ | I$_{OL}$ = 1.6 mA | | | 0.4 | V |
| V$_{DD}$ power supply current | I$_{DD}$ | | | | 30 | mA |
| V$_{PP}$ power supply current | I$_{PP}$ | MD0 = V$_{IL}$, MD1 = V$_{IH}$ | | | 30 | mA |

**Cautions 1. Avoid exceeding +13.5 V for V$_{PP}$ including the overshoot.**

**2. V$_{DD}$ must be applied before V$_{PP}$, and cut after V$_{PP}$.**

**AC PROGRAMMING CHARACTERISTICS (T$_A$ = 25 $\pm$ 5˚C, V$_{DD}$ = 6.0 $\pm$ 0.25 V, V$_{PP}$ = 12.5 $\pm$ 0.3 V, V$_{SS}$ = 0 V)**

| Parameter | Symbol | **Note 1** | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Address setup time [Note 2] (to MD0↓) | t$_{AS}$ | t$_{AS}$ | | 2 | | | $\mu$s |
| MD1 setup time (to MD0↓) | t$_{M1S}$ | t$_{OES}$ | | 2 | | | $\mu$s |
| Data setup time (to MD0↓) | t$_{DS}$ | t$_{DS}$ | | 2 | | | $\mu$s |
| Address hold time [Note 2] (from MD0↑) | t$_{AH}$ | t$_{AH}$ | | 2 | | | $\mu$s |
| Data hold time (from MD0↑) | t$_{DH}$ | t$_{DH}$ | | 2 | | | $\mu$s |
| MD0↑→data output float delay time | t$_{DF}$ | t$_{DF}$ | | 0 | | 130 | ns |
| V$_{PP}$ setup time (to MD3↑) | t$_{VPS}$ | t$_{VPS}$ | | 2 | | | $\mu$s |
| V$_{DD}$ setup time (to MD3↑) | t$_{VDS}$ | t$_{VCS}$ | | 2 | | | $\mu$s |
| Initial program pulse width | t$_{PW}$ | t$_{PW}$ | | 0.95 | 1.0 | 1.05 | ms |
| Additional program pulse width | t$_{OPW}$ | t$_{OPW}$ | | 0.95 | | 21.0 | ms |
| MD0 setup time (to MD1↑) | t$_{M0S}$ | t$_{CES}$ | | 2 | | | $\mu$s |
| MD0↓→data output delay time | t$_{DV}$ | t$_{DV}$ | MD0 = MD1 = V$_{IL}$ | | | 1 | $\mu$s |
| MD1 hold time (from MD0↑) | t$_{M1H}$ | t$_{OEH}$ | t$_{M1H}$ + t$_{M1R}$ ≥ 50 $\mu$s | 2 | | | $\mu$s |
| MD1 recovery time (from MD0↓) | t$_{M1R}$ | t$_{OR}$ | | 2 | | | $\mu$s |
| Program counter reset time | t$_{PCR}$ | – | | 10 | | | $\mu$s |
| X1 input high-/low-level width | t$_{XH}$, t$_{XL}$ | – | | 0.125 | | | $\mu$s |
| X1 input frequency | f$_X$ | – | | | | 4.19 | MHz |
| Initial mode set time | t$_I$ | – | | 2 | | | $\mu$s |
| MD3 setup time (to MD1↑) | t$_{M3S}$ | – | | 2 | | | $\mu$s |
| MD3 hold time (from MD1↓) | t$_{M3H}$ | – | | 2 | | | $\mu$s |
| MD3 setup time (to MD0↓) | t$_{M3SR}$ | – | During program memory read | 2 | | | $\mu$s |
| Address [Note 2] →data output delay time | t$_{DAD}$ | t$_{ACC}$ | During program memory read | | | 2 | $\mu$s |
| Address [Note 2] →data output hold time | t$_{HAD}$ | t$_{OH}$ | During program memory read | 0 | | 130 | ns |
| MD3 hold time (from MD0↑) | t$_{M3HR}$ | – | During program memory read | 2 | | | $\mu$s |
| MD3↓→data output float delay time | t$_{DFR}$ | – | During program memory read | | | 2 | $\mu$s |

**Notes 1.** Corresponding symbol of $\mu$PD27C256A

**2.** The internal address signal is incremented by 1 at the rising edge of the fourth X1 input and is not connected to the pin.
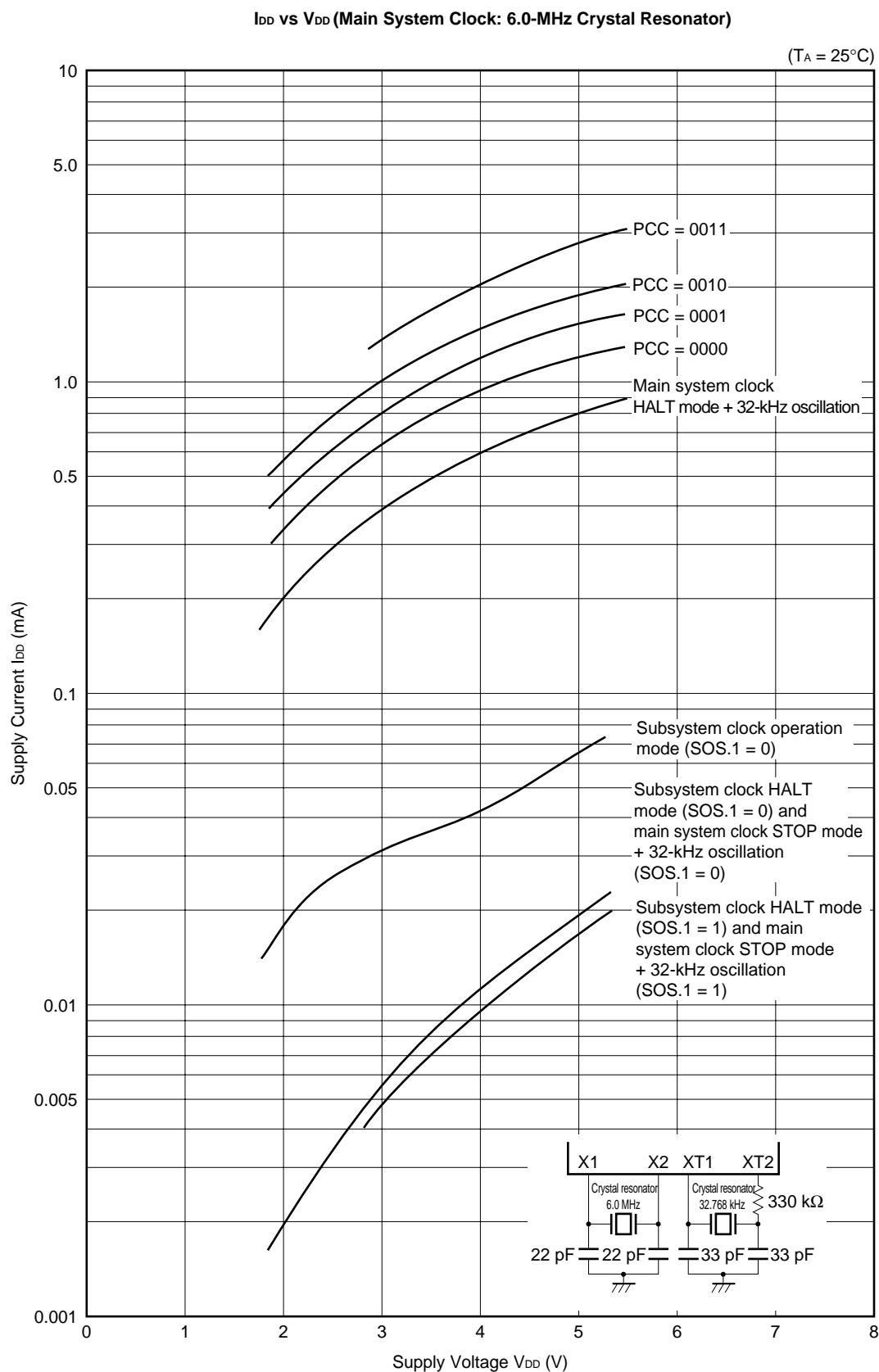
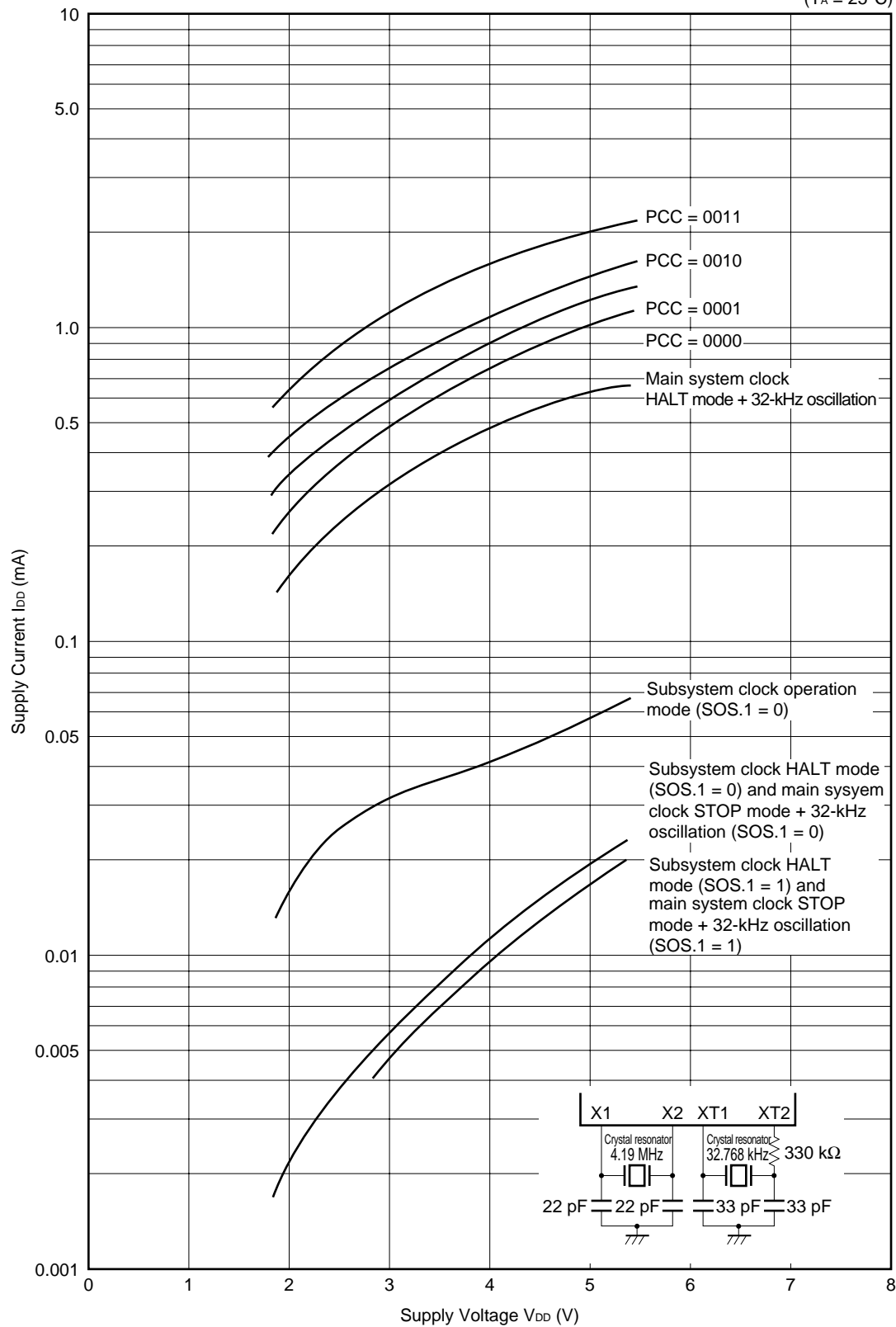**Program Memory Write Timing**
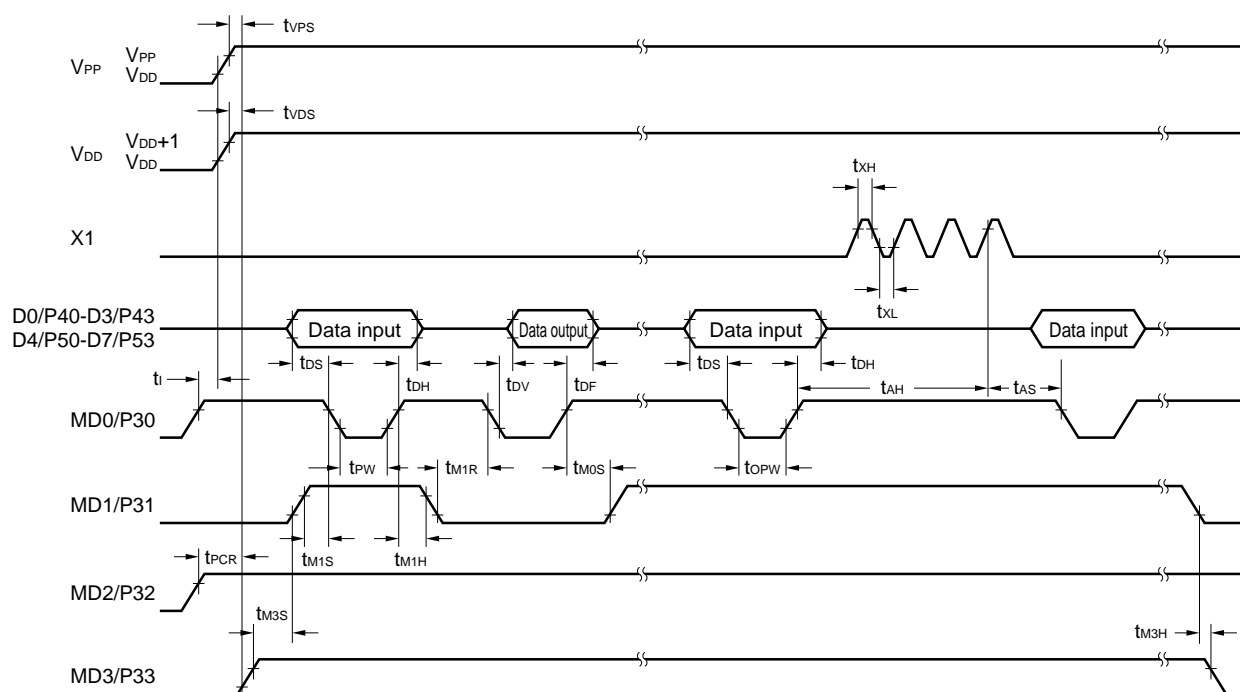


**Program Memory Read Timing**
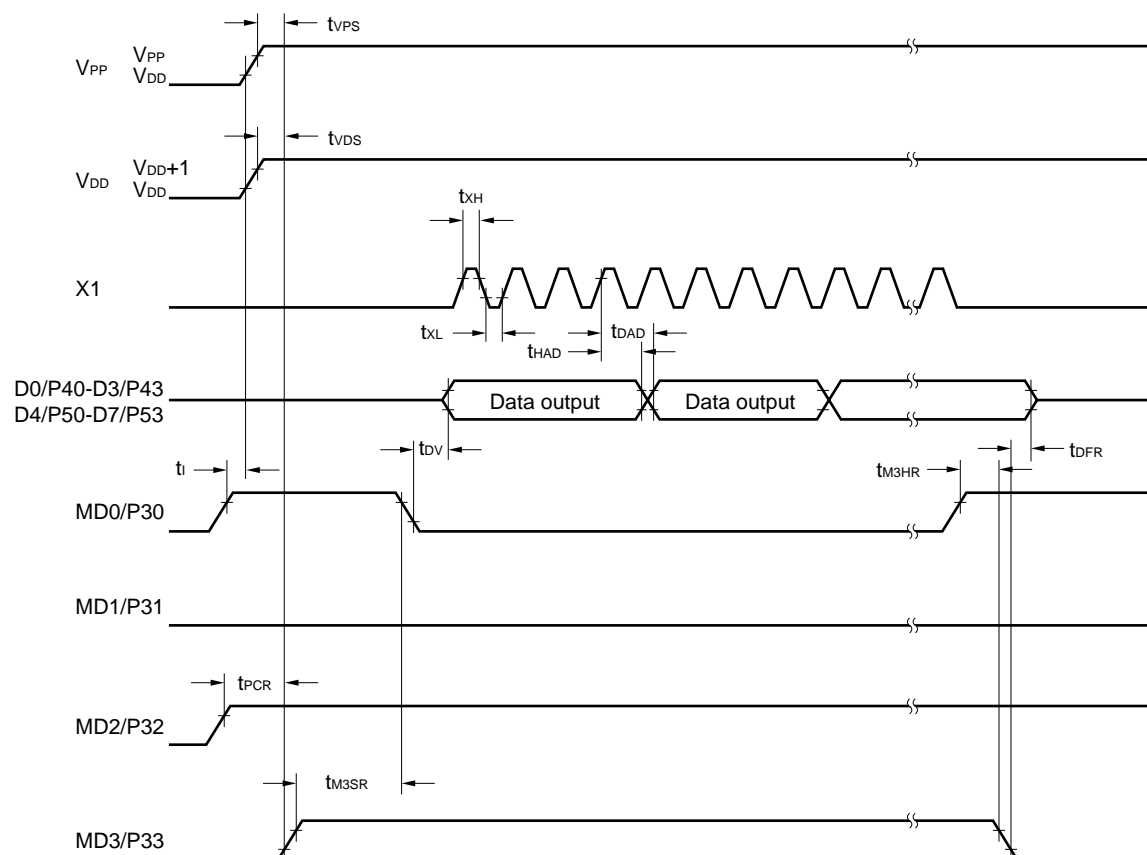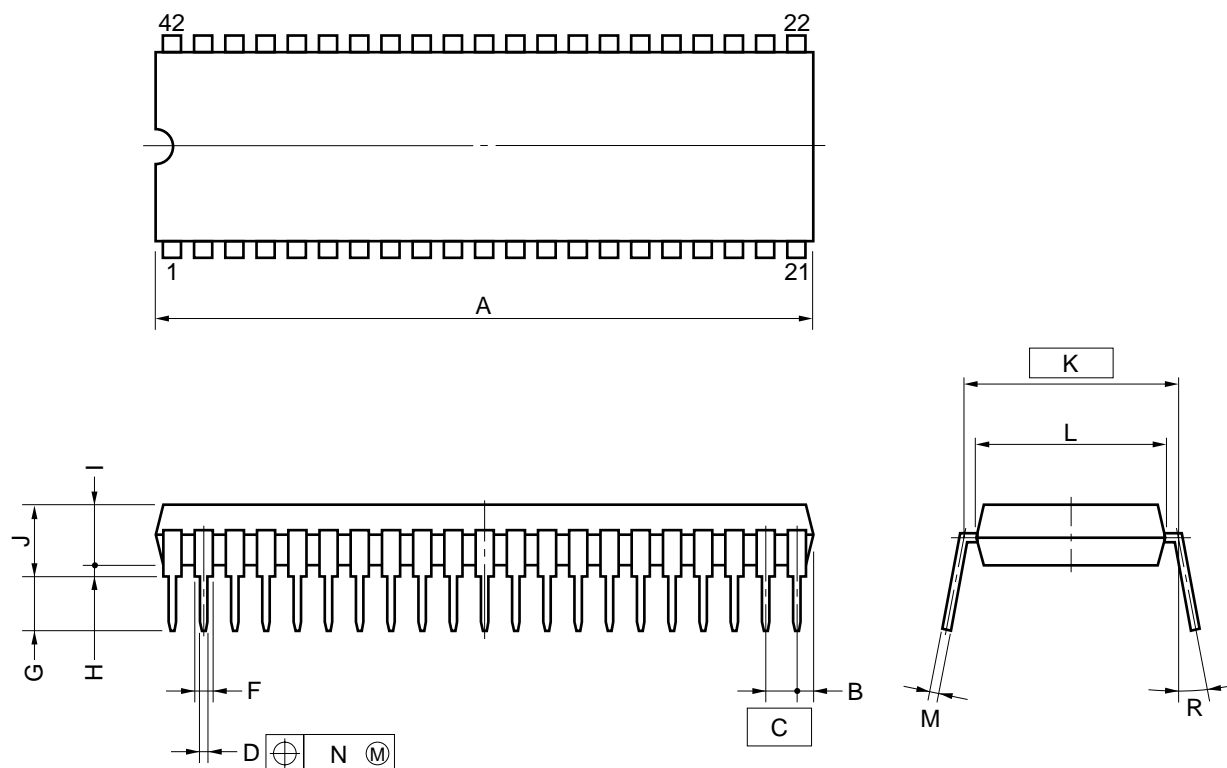
### 10. CHARACTERISTICS CURVES (REFERENCE VALUES)

**I$_{DD}$ vs V$_{DD}$ (Main System Clock: 6.0-MHz Crystal Resonator)**

(T$_A$ = 25°C)



PCC = 0011
PCC = 0010
PCC = 0001
PCC = 0000
Main system clock
HALT mode + 32-kHz oscillation

Subsystem clock operation mode (SOS.1 = 0)

Subsystem clock HALT mode (SOS.1 = 0) and main system clock STOP mode + 32-kHz oscillation (SOS.1 = 0)

Subsystem clock HALT mode (SOS.1 = 1) and main system clock STOP mode + 32-kHz oscillation (SOS.1 = 1)

X1   X2   XT1   XT2

Crystal resonator 6.0 MHz   Crystal resonator 32.768 kHz   330 kΩ

22 pF   22 pF   33 pF   33 pF

Supply Current I$_{DD}$ (mA)

Supply Voltage V$_{DD}$ (V)

**I_DD vs V_DD (Main System Clock: 4.19-MHz Crystal Resonator)**

$(T_A = 25°C)$



PCC = 0011

PCC = 0010

PCC = 0001

PCC = 0000

Main system clock
HALT mode + 32-kHz oscillation

Subsystem clock operation
mode (SOS.1 = 0)

Subsystem clock HALT mode
(SOS.1 = 0) and main sysyem
clock STOP mode + 32-kHz
oscillation (SOS.1 = 0)

Subsystem clock HALT
mode (SOS.1 = 1) and
main system clock STOP
mode + 32-kHz oscillation
(SOS.1 = 1)

X1        X2   XT1       XT2

Crystal resonator    Crystal resonator
4.19 MHz             32.768 kHz ⩾ 330 kΩ

22 pF — 22 pF    33 pF — 33 pF

Supply Current I_DD (mA)

Supply Voltage V_DD (V)

## 11. PACKAGE DRAWINGS

### 42PIN PLASTIC SHRINK DIP (600 mil)



**NOTES**

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|------|-------------|--------|
| A | 39.13 MAX. | 1.541 MAX. |
| B | 1.78 MAX. | 0.070 MAX. |
| C | 1.778 (T.P.) | 0.070 (T.P.) |
| D | 0.50±0.10 | $0.020^{+0.004}_{-0.005}$ |
| F | 0.9 MIN. | 0.035 MIN. |
| G | 3.2±0.3 | 0.126±0.012 |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 15.24 (T.P.) | 0.600 (T.P.) |
| L | 13.2 | 0.520 |
| M | $0.25^{+0.10}_{-0.05}$ | $0.010^{+0.004}_{-0.003}$ |
| N | 0.17 | 0.007 |
| R | 0~15° | 0~15° |

**P42C-70-600A-1**

**42 PIN PLASTIC SHRINK SOP (375 mil)**



detail of lead end
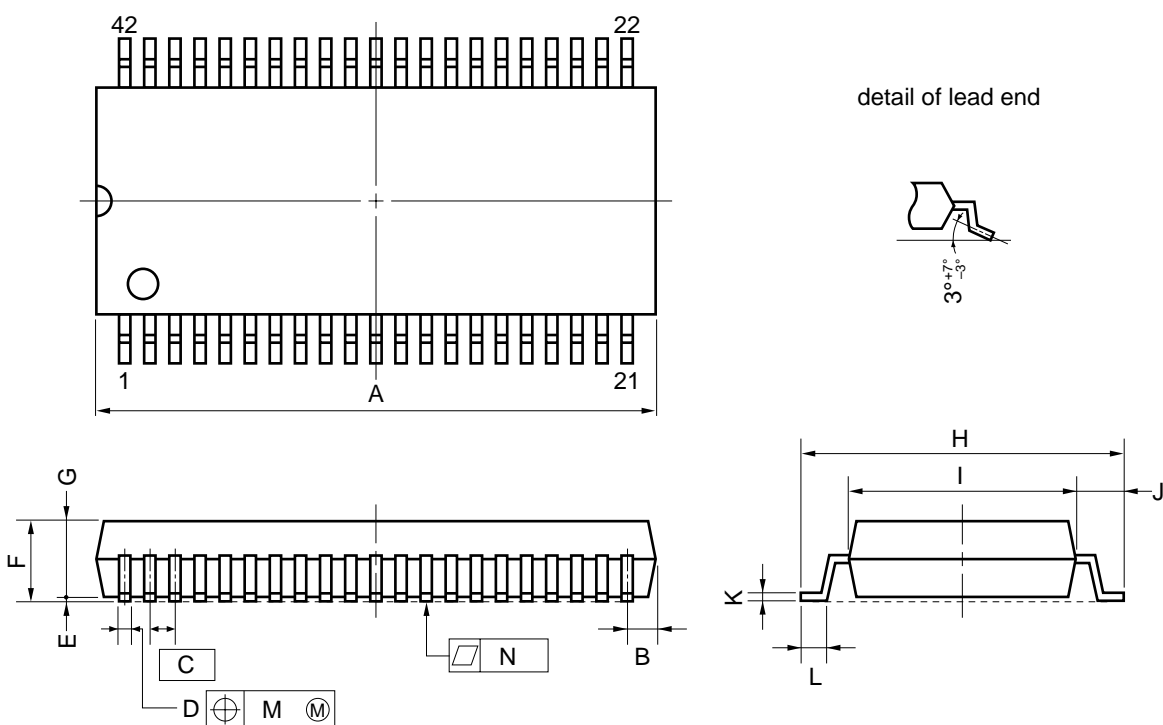
S42GT-80-375B-1

**NOTE**

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|-------------|--------|
| A | 18.16 MAX. | 0.715 MAX. |
| B | 1.13 MAX. | 0.044 MAX. |
| C | 0.8 (T.P.) | 0.031 (T.P.) |
| D | $0.35^{+0.10}_{-0.05}$ | $0.014^{+0.004}_{-0.003}$ |
| E | 0.125±0.075 | 0.005±0.003 |
| F | 2.9 MAX. | 0.115 MAX. |
| G | 2.5±0.2 | $0.098^{+0.009}_{-0.008}$ |
| H | 10.3±0.3 | $0.406^{+0.012}_{-0.013}$ |
| I | 7.15±0.2 | $0.281^{+0.009}_{-0.008}$ |
| J | 1.6±0.2 | 0.063±0.008 |
| K | $0.15^{+0.10}_{-0.05}$ | $0.006^{+0.004}_{-0.002}$ |
| L | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| M | 0.10 | 0.004 |
| N | 0.10 | 0.004 |

★ ## 12. RECOMMENDED SOLDERING CONDITIONS

The *μ*PD75P0076 should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC Sales representative.

### Table 12-1.  Surface Mounting Type Soldering Conditions

*μ*PD75P0076GT:  42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235˚C, Time: 30 seconds or less (at 210˚C or higher), Number of reflow processes: Twice or less | IR35-00-2 |
| VPS | Package peak temperature: 215˚C, Time: 40 seconds or less (at 200˚C or higher), Number of reflow processes: Twice or less | VP15-00-2 |
| Wave soldering | Solder temperature: 260˚C or below, Time: 10 seconds or less, Number of flow process: 1, Preheating temperature: 120˚C or below (Package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300˚C or below, Time : 3 seconds or less (per device side) | — |

**Caution   Use of more than one soldering method should be avoided (except for partial heating).**

### Table 12-2.  Insertion Type Soldering Conditions

*μ*PD75P0076CU:  42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)

| Soldering Method | Soldering Conditions |
|---|---|
| Wave soldering (pins only) | Solder bath temperature:  260 ˚C or less, Time:  10 seconds or less |
| Partial heating | Pin temperature:  300 ˚C or below, Time:  3 seconds or less (per device side) |

**Caution   Ensure that the application of wave soldering is limited to the pins and no solder touches the main unit directly.**

## APPENDIX A   DIFFERENCES AMONG μPD75068, 750068 AND 75P0076

| Parameter | | μPD75068 | μPD750068 | μPD75P0076 |
|---|---|---|---|---|
| Program memory | | Mask ROM<br>0000H to 1F7FH<br>(8064 x 8 bits) | Mask ROM<br>0000H to 1FFFH<br>(8192 x 8 bits) | One-time PROM<br>0000H to 3FFFH<br>(16384 x 8 bits) |
| Data memory | | 000H to 1FFH<br>(512 x 4 bits) | | |
| CPU | | 75X Standard CPU | 75XL CPU | |
| General-purpose register | | 4 bits x 8 or 8 bits x 4 | (4 bits x 8 or 8 bits x 4) x 4 banks | |
| Instruction execution time | When main system clock is selected | 0.95, 1.91, 15.3 μs<br>(during 4.19-MHz operation) | • 0.67, 1.33, 2.67, 10.7 μs (during 6.0-MHz operation)<br>• 0.95, 1.91, 3.81, 15.3 μs (during 4.19-MHz operation) | |
| | When subsystem clock is selected | 122 μs (during 32.768-kHz operation) | | |
| I/O port | CMOS input | 12 (Connections of on-chip pull-up resistor specified by software: 7) | | |
| | CMOS input/output | 12 (Connections of on-chip pull-up resistor specified by software) | | |
| | N-ch open-drain input/output | 8 (on-chip pull-up resistor specified by mask option)<br>Withstand voltage is 10 V | 8 (on-chip pull-up resistor specified by mask option)<br>Withstand voltage is 13 V | 8 (no mask option)<br>Withstand voltage is 13 V |
| | Total | 32 | | |
| Timer | | 3 channels<br>• 8-bit timer/event counter<br>• 8-bit basic interval timer<br>• Watch timer | 4 channels<br>• 8-bit timer/event counter 0 (watch timer output added)<br>• 8-bit timer/event counter 1 (can be used as a 16-bit timer/<br>  event counter)<br>• 8-bit basic interval timer/watchdog timer<br>• Watch timer | |
| A/D converter | | • 8-bit resolution x 8 channels<br>  (successive approximation)<br>• Can operate at the voltage<br>  from $V_{DD}$ = 2.7 V | • 8-bit resolution x 8 channels<br>  (successive approximation)<br>• Can operate at the voltage from $V_{DD}$ = 1.8 V | |
| Clock output (PCL) | | Φ, 524, 262, 65.5 kHz<br>(Main system clock:<br>during 4.19-MHz operation) | • Φ, 1.05 MHz, 262 kHz, 65.5 kHz<br>  (Main system clock: during 4.19-MHz operation)<br>• Φ, 1.5 MHz, 375 kHz, 93.8 kHz<br>  (Main system clock: during 6.0-MHz operation) | |
| Buzzer output (BUZ) | | 2, 4, 32 kHz<br>(Main system clock:<br>during 4.19-MHz operation<br>or subsystem clock: during<br>32.768-kHz operation) | • 2, 4, 32 kHz<br>  (Main system clock: during 4.19-MHz operation or<br>  subsystem clock: during 32.768-kHz operation)<br>• 2.93, 5.86, 46.9 kHz<br>  (Main system clock: during 6.0-MHz operation) | |
| Serial interface | | 3 modes supported<br>• 3-wire serial I/O mode<br>  ...MSB/LSB first selectable<br>• 2-wire serial I/O mode<br>• SBI mode | 2 modes supported<br>• 3-wire serial I/O mode...MSB/LSB first selectable<br>• 2-wire serial I/O mode | |
| Vectored interrupt | | 3 external, 3 internal | 3 external, 4 internal | |
| Test inputs | | 1 external, 1 internal | | |
| Power supply voltage | | $V_{DD}$ = 2.7 to 6.0 V | $V_{DD}$ = 1.8 to 5.5 V | |
| Operating ambient temperature | | $T_A$ = −40 to +85 °C | | |
| Package | | • 42-pin plastic shrink DIP<br>  (600 mil)<br>• 44-pin plastic QFP<br>  (10 x 10 mm) | • 42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)<br><br>• 42-pin plastic shrink SOP (375 mil, 0.8-mm pitch) | |

**Note** Under development

## APPENDIX B   DEVELOPMENT TOOLS

The following development tools are provided for system development using the $\mu$PD75P0076.  In the 75XL series, the common relocatable assembler of the series is used together with device files according to the product.

| RA75X relocatable assembler | Host machine | | | Order code (Part No.) |
|---|---|---|---|---|
| | | OS | Supply Medium | |
| | PC-9800 Series | MS-DOS™ | 3.5" 2HD | $\mu$S5A13RA75X |
| | | Ver.3.30 to Ver.6.2**Note** | 5" 2HD | $\mu$S5A10RA75X |
| | IBM PC/AT™ | Refer to **OS for** | 3.5" 2HC | $\mu$S7B13RA75X |
| | or compatible | **IBM PCs** | 5" 2HC | $\mu$S7B10RA75X |

| Device file | Host machine | | | Order code (Part No.) |
|---|---|---|---|---|
| | | OS | Supply Medium | |
| | PC-9800 Series | MS-DOS | 3.5" 2HD | $\mu$S5A13DF750068 |
| | | Ver.3.30 to Ver.6.2**Note** | 5" 2HD | $\mu$S5A10DF750068 |
| | IBM PC/AT | Refer to **OS for** | 3.5" 2HC | $\mu$S7B13DF750068 |
| | or compatible | **IBM PCs** | 5" 2HC | $\mu$S7B10DF750068 |

**Note**   Ver. 5.00 or later include a task swapping function, but this software is not able to use that function.

**Remark**   Operation of the assembler and device file is guaranteed only when using the host machine and OS described above.

### PROM Write Tools

| Hardware | PG-1500 | This is a PROM programmer which enables you to program a single-chip microcontroller with on-chip PROM by stand-alone or host machine operation by connecting an attached board and a programmer adapter (sold separately).<br>In addition, typical PROMs in capacities ranging from 256 K to 4 M bits can be programmed. | | | |
|---|---|---|---|---|---|
| | PA-75P0076CU | This is a PROM programmer adapter dedicated for the $\mu$PD75P0076CU and 75P0076GT.  It can be used when connected to a PG-1500. | | | |
| Software | PG-1500 controller | PG-1500 and a host machine are connected by serial and parallel interfaces and PG-1500 is controlled on the host machine. | | | |
| | | Host machine | | | Order code (Part No.) |
| | | | OS | Supply medium | |
| | | PC-9800 Series | MS-DOS | 3.5" 2HD | $\mu$S5A13PG1500 |
| | | | Ver.3.30 to Ver.6.2**Note** | 5" 2HD | $\mu$S5A10PG1500 |
| | | IBM PC/AT | Refer to **OS for** | 3.5" 2HD | $\mu$S7B13PG1500 |
| | | or compatible | **IBM PCs** | 5" 2HC | $\mu$S7B10PG1500 |

**Note**   Ver. 5.00 or later include a task swapping function, but this software is not able to use that function.

**Remark**   Operation of the PG-1500 controller is guaranteed only when using the host machine and OS described above.

**Debugging Tools**

In-circuit emulators (IE-75000-R and IE-75001-R) are provided as program debugging tools for the $\mu$PD75P0076.

Various system configurations using these in-circuit emulators are listed below.

| | | |
|---|---|---|
| Hardware | IE-75000-R**Note 1** | The IE-75000-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems that use 75X or 75XL Series products.  For development of the $\mu$PD750068 subseries, the IE-75000-R is used with a separately sold emulation board (IE-75300-R-EM) and emulation probe.<br>These products can be applied for highly efficient debugging when connected to a host machine and PROM programmer.<br>The IE-75000-R can include a connected emulation board (IE-75000-R-EM). |
| | IE-75001-R | The IE-75001-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems that use 75X or 75XL Series products.  The IE-75001-R is used with a separately sold emulation board (IE-75300-R-EM) and emulation probe.<br>These products can be applied for highly efficient debugging when connected to a host machine and PROM programmer. |
| | IE-75300-R-EM | This is an emulation board for evaluating application systems that use the $\mu$PD750068 subseries.  It is used in combination with the IE-75000-R or IE-75001-R in-circuit emulator. |
| | EP-750068CU-R | This is an emulation probe for the $\mu$PD75P0076CU.<br>When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM. |
| | EP-750068GT-R | This is an emulation probe for the $\mu$PD75P0076GT. |
| | EV-9500GT-42 | When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM. It includes a flexible board (EV-9500GT-42) to facilitate connections with target systems. |
| Software | IE control program | This program can control the IE-75000-R or IE-75001-R on a host machine when connected to the IE-75000-R or IE-75001-R via an RS-232-C or Centronics interface. |

| Host machine | | | Order code (Part No.) |
|---|---|---|---|
| | OS | Supply Medium | |
| PC-9800 Series | MS-DOS | 3.5" 2HD | $\mu$S5A13IE75X |
| | $\left(\begin{array}{c}\text{Ver.3.30 to}\\\text{Ver.6.2}^{\textbf{Note 2}}\end{array}\right)$ | 5" 2HD | $\mu$S5A10IE75X |
| IBM PC/AT | Refer to **OS for** | 3.5" 2HC | $\mu$S7B13IE75X |
| or compatible | **IBM PCs** | 5" 2HC | $\mu$S7B10IE75X |

**Notes 1.** This is a service part provided for maintenance purpose only.

**2.** Ver. 5.00 or later include a task swapping function, but this software is not able to use that function.

**Remarks 1.** Operation of the IE control program is guaranteed only when using the host machine and OS described above.

**2.** The generic name for the $\mu$PD750064, 750066, 750068, and 75P0076 is the $\mu$PD750068 subseries.

### OS for IBM PCs

The following operating systems for the IBM PC are supported.

| OS | Version |
|---|---|
| PC DOS™ | Ver.5.02 to Ver.6.3<br>J6.1/V[Note] to J6.3/V[Note] |
| MS-DOS | Ver.5.0 to Ver.6.22<br>5.0/V[Note] to 6.2/V[Note] |
| IBM DOS™ | J5.02/V[Note] |

**Note**   Only the English mode is supported.

**Caution    Ver 5.0 and above include a task swapping function, but this software is not able to use that function.**

★ **APPENDIX C RELATED DOCUMENTS**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

**Documents related to device**

| Document Name | Document No. | |
|---|---|---|
| | English | Japanese |
| $\mu$PD750064, 750066, 750068, 750064(A), 750066(A), 750068(A) Data Sheet | U10165E**Note** | U10165J |
| $\mu$PD75P0076 Data Sheet | This document | U10232J |
| $\mu$PD750068 User's Manual | U10670E | U10670J |
| $\mu$PD750068 Instruction Table | — | IEM-5606 |
| 75XL Series Selection Guide | U10453E | U10453J |

**Note** Preliminary product information

**Documents related to development tool**

| Document Name | | | Document No. | |
|---|---|---|---|---|
| | | | English | Japanese |
| Hardware | IE-75000-R/IE-75001-R User's Manual | | EEU-1416 | EEU-846 |
| | IE-75300-R-EM User's Manual | | U11345E | U11354J |
| | EP-750068GT-R User's Manual | | U10950E | U10950J |
| | PG-1500 User's Manual | | EEU-1335 | EEU-651 |
| Software | RA75X Assembler Package User's Manual | Operation | EEU-1346 | EEU-731 |
| | | Language | EEU-1363 | EEU-730 |
| | PG-1500 Controller User's Manual | PC-9800 Series (MS-DOS) base | EEU-1291 | EEU-704 |
| | | IBM PC Series (PC DOS) base | U10540E | EEU-5008 |

**Other related documents**

| Document Name | Document No. | |
|---|---|---|
| | English | Japanese |
| IC Package Manual | C10943X | |
| Semiconductor Device Mounting Technology Manual | C10535E | C10535J |
| NEC Semiconductor Device Quality Grades | C11531E | C11531J |
| NEC Semiconductor Device Reliability and Quality Control | C10983E | C10983J |
| Electrostatic Discharge (ESD) Test | — | MEM-539 |
| Semiconductor Device Quality Assurance Guide | MEI-1202 | MEI-603 |
| Microcontroller-related Product Guide —Third Party Products— | — | U11416J |

**Caution The contents of the documents listed above are subject to change without prior notice to users. Make sure to use the latest edition when starting design.**

[MEMO]

## NOTES FOR CMOS DEVICES

### (1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### (2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### (3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

# Regional Information

Some information contained in this document may vary from country to country.  Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors.  They will verify:

• Device availability

• Ordering information

• Product release schedule

• Availability of related technical literature

• Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)

• Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

**NEC Electronics Inc. (U.S.)**
Santa Clara, California
Tel: 800-366-9782
Fax: 800-729-9288

**NEC Electronics (Germany) GmbH**
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

**NEC Electronics (UK) Ltd.**
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

**NEC Electronics Italiana s.r.1.**
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

**NEC Electronics (Germany) GmbH**
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

**NEC Electronics (France) S.A.**
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

**NEC Electronics (France) S.A.**
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

**NEC Electronics (Germany) GmbH**
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

**NEC Electronics Hong Kong Ltd.**
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

**NEC Electronics Hong Kong Ltd.**
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

**NEC Electronics Singapore Pte. Ltd.**
United Square, Singapore 1130
Tel: 253-8311
Fax: 250-3583

**NEC Electronics Taiwan Ltd.**
Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

**NEC do Brasil S.A.**
Sao Paulo-SP, Brasil
Tel: 011-889-1680
Fax: 011-889-1689

**J96. 8**

**MS-DOS is a trademark of Microsoft Corporation.**

**PC DOS, PC/AT, and IBM DOS are trademarks of IBM Corporation.**

The export of this product from Japan is regulated by the Japanese government.  To export this product may be prohibited without governmental license, the need for which must be judged by the customer.  The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country.  Please call an NEC sales representative.