DESCRIPTION

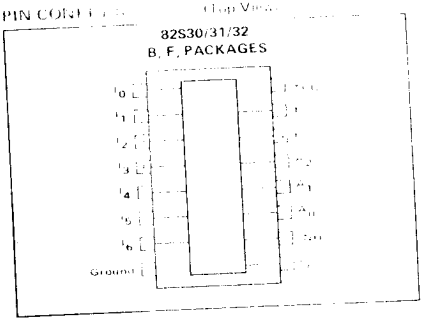
These 8-Input Digital Multiplexers are the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 82S30 incorporates an INHIBIT input which, when low, allows the one-of-eight inputs selected by the address to appear on the f output and, in complement, on the f output. With the INHIBIT input high, the f output is unconditionally low and the f output is unconditionally high. The 82S31 is a variation of the 82S30 that provides an open collector output f for expansion of input terms.

The 82S32 is similar to the 82S30 except in the effect of the INHIBIT input on the f output. With the INHIBIT low, the selected input appears at the f output and, in complement, on the f output. With the INHIBIT input high, both the f and the f output are unconditionally low.

PIN CONFIGURATION (Top View)

82S30/31/32
B, F, PACKAGES

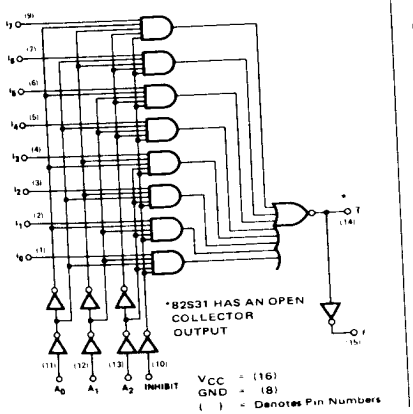


FEATURES

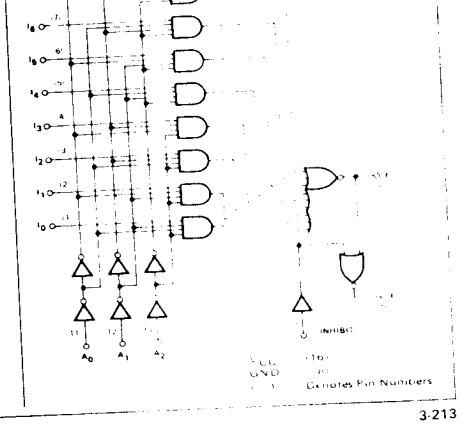
- SCHOTTKY-CLAMPED TTL STRUCTURE
- LOW CURRENT PNP INPUTS
- 82S30 REPLACES 9312 FOR HIGHER SPEED
- 82S31 HAS OPEN COLLECTOR OUTPUT
- 82S32 HAS DIRECT OUTPUT INHIBIT

LOGIC DIAGRAMS

82S30/82S31



82S32



D.C. ELECTRICAL CHARACTERISTICS Over Recommended Operating Temperature and Voltage

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN	TYP	MAX	UNITS	A_1	A_2	A_3	INH	DATA INPUT I_n	OUTPUTS	
"I" Output Voltage (All outputs except $\overline{f}$ of 82S31)	2.7			V	*	*	*	*		−1.0mA	6,10
"I" Output Leakage Current			250	μA	*	*	*	*			
"O" Output Voltage			0.5	V	*	*	*	*		20mA	7,10
"I" Input Current Inputs An, In, Inh			10	μA	4.5V	4.5V	4.5V	4.5V	4.5V		
"0" Input Current A_n, I_n, INH			−400	μA	0.5V	0.5V	0.5V	0.5V	0.5V		
Power Consumption/ Supply Current			325/62	mW/mA	4.5V	4.5V	4.5V	4.5V	0V		9,11
Output Short Circuit Current Output f	−40		−100	mA	0V	0V	0V	0V	4.5V	0V	9
Output $\overline{f}$	−40		−100	mA	0V	0V	0V	0V	0V	0V	9
Input Clamp Voltage	−1.2			V	−18 mA	−18 mA	−18 mA	−18 mA			

*See Truth Table for logical conditions.

A.C. ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS		LIMITS				TEST CONDITIONS	NOTES
		MIN	TYP	MAX	UNITS		
Propagation Delay (t_{on},t_{off})							
Data, I_n to $\overline{f}$	82S30/32		7	10	ns		
	82S31		9	12	ns		
Address A_n to $\overline{f}$	82S30/32		14	17	ns	Per Test Table	
	82S31		16	19	ns	$R_L = 280\Omega$	8
$\overline{f}$ to $\overline{f}$			6	9	ns	$C_L = 15pF$	
INH to $\overline{f}$	82S30/32		12	16	ns		
	82S31		14	18	ns		

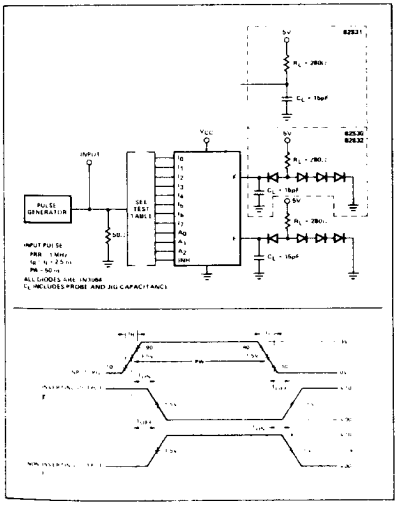
NOTES
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures.
9. $V_{CC} = 5.25V$.
10. By DC tests per the truth table, all inputs have guaranteed thresholds at 0.8V for logical "0" and 2.0V for logical "1".
11. All I_n data inputs are at 0V.

TRUTH TABLE

ADDRESS			DATA INPUT										OUTPUTS	
A_2	A_1	A_0	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	INH	t	t 82S30/31	$\overline{t}$ 82S32
0	0	0	X	X	X	X	X	X	X	1	0	1	0	0
0	0	1	X	X	X	X	X	X	1	X	0	1	0	0
0	1	0	X	X	X	X	X	1	X	X	0	1	0	0
0	1	1	X	X	X	X	1	X	X	X	0	1	0	0
1	0	0	X	X	X	1	X	X	X	X	0	1	0	0
1	0	1	X	X	1	X	X	X	X	X	0	1	0	0
1	1	0	X	1	X	X	X	X	X	X	0	1	0	0
1	1	1	1	X	X	X	X	X	X	X	0	1	0	0
0	0	0	X	X	X	X	X	X	X	0	0	0	1	1
0	0	1	X	X	X	X	X	X	0	X	0	0	1	1
0	1	0	C	X	X	X	X	0	X	X	0	0	1	1
0	1	1	X	X	X	X	0	X	X	X	0	0	1	1
1	0	0	X	X	X	0	X	X	X	X	0	0	1	1
1	0	1	X	X	0	X	X	X	X	X	0	0	1	1
1	1	0	X	0	X	X	X	X	X	X	0	0	1	1
1	1	1	0	X	X	X	X	X	X	X	0	0	1	1
X	X	X	C	X	X	X	X	X	X	X	1	0	1	0

X = don't care

A.C. TEST FIGURE AND WAVEFORMS



TEST TABLE

TEST NO.	INPUTS											OUTPUTS	
	A_0	A_1	A_2	INH	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	F	F
1	PG	0	0	0	0	1	0	0	0	0	0	0	T	T
2	0	PG	0	0	0	0	1	0	0	0	0	0	T	
3	0	0	PG	0	0	0	0	0	1	0	0	0	T	
4	0	1	1	PG	0	0	0	0	0	1	0	0	T	
5	1	1	1	0	0	0	0	0	0	0	0	PG	T	

F: "H" = 2.7V "0" = GROUND

NOTE

1. AC test jigs must not have any switches.
2. AC test jigs must have less than 1.8 inch lead lengths from package pins.