19-1342; Rev 1; 8/98

EVALUATION KIT AVAILABLE

0.1%-Accurate Signal Conditioner for Piezoresistive Sensor Compensation

General Description

The MAX1457 is a highly integrated analog-sensor signal processor optimized for piezoresistive sensor calibration and compensation. It includes a programmable current source for sensor excitation, a 3-bit programmable-gain amplifier (PGA), a 12-bit ADC, five 16-bit DACs, and an uncommitted op amp. Achieving a total error factor within 0.1% of the sensor's repeatability errors, the MAX1457 compensates offset, full-span output (FSO), offset TC, FSO TC, and full-span output nonlinearity of silicon piezoresistive sensors.

The MAX1457 calibrates and compensates first-order temperature errors by adjusting the offset and span of the input signal via digital-to-analog converters (DACs), thereby eliminating quantization noise. If needed, residual higher-order errors are then compensated using linear interpolation of the first-order coefficients stored in a look-up table (in external EEPROM).

The MAX1457 integrates three traditional sensormanufacturing operations into one automated process:

- Pretest: Data acquisition of sensor performance under the control of a host test computer.
- Calibration and Compensation: Computation and storage (in an external EEPROM) of calibration and compensation coefficients determined from transducer pretest data.
- Final Test: Verification of transducer calibration and compensation, without removal from a pretest socket.

Analog outputs are provided for both pressure and temperature. A general-purpose, uncommitted op amp is also included on-chip to increase the overall circuit gain, or to facilitate the implementation of a 2-wire, 4–20mA transmitter. The serial interface is compatible with MicroWire[™] and SPI[™], and directly connects to an external EEPROM. Additionally, built-in testability features of the MAX1457 facilitate manufacturing and calibration of multiple sensor modules, thus lowering manufacturing cost.

Although optimized for use with piezoresistive sensors, the MAX1457 may also be used with other resistive sensor types (i.e., accelerometers and strain gauges) with the addition of a few external components.

Customization

Maxim can customize the MAX1457 for unique requirements. With a dedicated cell library of more than 90 sensor-specific functional blocks, Maxim can quickly provide customized MAX1457 solutions. Contact Maxim for additional information.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd. SPI is a trademark of Motorola, Inc. MicroWire is a trademark of National Semiconductor Corp.

_Features

- High Accuracy (within ±0.1% of sensor's repeatable errors)
- Compensates Offset, Offset TC, FSO, FSO TC, Temperature/Pressure Nonlinearity

MXXIM

- Rail-to-Rail[®] Analog Output for Calibrated, Temperature-Compensated Pressure Measurements
- Programmable Sensor Excitation Current
- ♦ SPI/MicroWire-Compatible Serial Interface
- Fast Signal-Path Settling Time (<1ms)</p>
- ♦ Accepts Sensor Outputs from 5mV/V to 30mV/V
- Pin-Compatible with MCA7707

_Ordering Information

Functional Diagram

PART	TEMP. RANGE	PIN-PACKAGE
MAX1457CWI	0°C to +70°C	28 Wide SO
MAX1457CCJ	0°C to +70°C	32 TQFP
MAX1457C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet. Note: Contact the factory for customized solutions. *Dice are tested at $T_A = +25^{\circ}C$.

Pin Configurations appear at end of data sheet.

VDD BIAS NBIAS GENERATOR ISRC Ŕ MAX1457 FADJ OSCILLATOR - FOUT BDRIVE INP PGA VOUT - I INDAC INM V_{DD} - FSOTCDAC - OTCDAC \leq AGND OFSTDAC - FSODAC 12-BIT ADC - LINOUT FSO Ч MCS FSOTCOUT DAC ECS SERIAL VBDRIVE EEPROM 16-BIT 16-BIT 16-BIT 16-BIT 16-BIT A = 1 ECLK INTERFACE EDI VBBUF FDO LINDACREF -AMP+ -AMPOUT AMP-Vss

M/IXI/M

Maxim Integrated Products 1

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to V_{SS}.....-0.3V to +6V All other pins(V_{SS} - 0.3V) to (V_{DD} + 0.3V) Continuous Power Dissipation ($T_A = +70^{\circ}$ C)

28-Pin Wide SO (derate 12.50mW/°C above +70°C)1W 32-Pin TQFP (derate 11.1mW/°C above +70°C).......889mW

Operating Temperature Ranges

MAX1457C	0°C to +70°C
MAX1457A	40°C to +125°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP MAX	UNITS
GENERAL CHARACTERISTICS	;	1			1
Supply Voltage	V _{DD}		4.5	5 5.5	V
Supply Current	IDD	$R_{BIAS} = 400k\Omega$, $f_{CLK} = 100kHz$ (Note 1)		2.0 2.6	mA
ANALOG INPUT (PGA)	1	1	1		1
Input Impedance	RIN			1	MΩ
Input-Referred Offset Tempco		(Notes 2, 3)	:	±0.5	µV/°C
Amplifier Gain Nonlinearity			0.01		%V _{DD}
Output Step-Response Time		f _{CLK} = 100kHz, to 63% of final value		1	ms
Common-Mode Rejection Ratio	CMRR	From V _{SS} to V _{DD}		90	dB
Input-Referred Adjustable Offset Range		(Note 4)	±100		mV
Input-Referred Adjustable Full-Span Output Range		(Note 5)	5 to 30		mV/V
ANALOG OUTPUT (PGA)	1				1
Differential Signal Gain Range			54	to 306	V/V
Minimum Differential Signal Gain		$T_A = T_{MIN}$ to T_{MAX}	49	54 60	V/V
Differential Signal Gain Tempco				±50	ppm/°C
Output Voltage Swing		5k Ω load to V _{SS} or V _{DD}	V _{SS} + 0.25	V _{DD} - 0.25	V
Output voltage Swing		No load	$V_{SS} + 0.02$	V _{DD} - 0.02	v
Output Current Range		$V_{OUT} = (V_{SS} + 0.25V)$ to $(V_{DD} - 0.25V)$	-1.0 (sink)	1.0 (source)	mA
Output Noise		Gain = 54, DC to 10Hz, sensor impedance = $5k\Omega$, full-span output = 4V	0.0025		%FSO
CURRENT SOURCE	1				1
Bridge Current Range	IBR		0.1	0.5 2.0	mA
Bridge Voltage Swing	V _{BR}		V _{SS} + 1.3	V _{DD} - 1.3	V
Current-Source Reference Input Voltage Range	VISRC		V _{SS} + 1.3	V _{DD} - 1.3	V
DIGITAL-TO-ANALOG CONVER	RTERS	1	1		1
DAC Voltage Resolution		Reference voltage = 5.000V		200	μV
Differential Nonlinearity		Output filter capacitor = 0.1µF, f _{CLK} = 100kHz	z 2		LSB
DAC Resolution				16	Bits

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN T	YP MAX	UNITS	
ANALOG-TO-DIGITAL CONVE	RTER				1	
ADC Differential Nonlinearity		$V_{BR} = 2.5V$ to 3.5V, $f_{CLK} = 100$ kHz		2	LSB	
Conversion Time		f _{CLK} = 100kHz	1	60	ms	
ADC Resolution				12	Bits	
OUTPUTS (LINDAC, FSOTCDA	AC)	-				
Voltage Swing		$R_{BIAS} = 400 k \Omega$ (no load)	V _{SS} + 1.3	V _{DD} - 1.3	V	
Current Drive		$ R_{BIAS} = 400 k \Omega, \ V_{IN} = 2.5 V, \\ V_{OUT} = 2.5 V \pm 20 m V $	-50	50	μA	
Offset Voltage	Vofs	$(V_{IN} - V_{OUT})$ at $V_{IN} = 2.5V$, R _{BIAS} = 400k Ω (no load)	-20	20	mV	
UNCOMMITTED OP AMP			·			
Input Common-Mode Voltage Range	CMR		V _{SS} + 1.3	V _{DD} - 1.2	V	
Open-Loop Gain	Av	$R_{BIAS} = 400 k \Omega$	60		dB	
Offset Voltage (as unity-gain follower)		$R_{BIAS} = 400k\Omega$, $V_{IN} = 2.5V$ (no load)	-20	20	mV	
Output Voltago Swipg		5k Ω load to V _{SS} or V _{DD}	V _{SS} + 0.25	V _{DD} - 0.25	V	
Output Voltage Swing		No load	V _{SS} + 0.02	V _{DD} - 0.02		
Output Current Range		Vout = (Vss + 0.25V) to (V _{DD} - 0.25V)	-1.0 (sink)	1.0 (source)	mA	

Note 1: Circuit of Figure 5 with current source turned off. This value is adjustable through a bias resistor and represents the IC current consumption. This excludes the 93C66 EEPROM average current, which is approximately 13µA at a refresh rate of 3Hz (f_{CLK} = 100kHz).

Note 2: Temperature errors for the entire range are compensated together with the sensor errors.

Note 3: The sensor and the MAX1457 must always be at the same temperature during calibration and use.

Note 4: This is the maximum allowable sensor offset at minimum gain (54V/V).

Note 5: This is the sensor's sensitivity normalized to its drive voltage, assuming a desired full-span output of 4V and a bridge voltage of 2.5V. Lower sensitivities can be accommodated by using the auxiliary op amp. Higher sensitivities can be accommodated by operating at lower bridge voltages.

_Pin Description

S0 TGFP Positive Sensor Input. Input impedance > 1MΩ. Rail-to-rail input range. 1 28 INP Positive Sensor Input. Input impedance > 1MΩ. Rail-to-rail input range. 2 29 INM Negative Sensor Input. Input impedance > 1MΩ. Rail-to-rail input range. 3 30 AMP+ Positive Input of General-Purpose Operational Amplifier 4 31 AMP- Negative Input of General-Purpose Operational Amplifier 6 2 BDRIVE Sensor Excitation Current. This pin drives a nominal 0.5mA through the sensor. 7 3 VOUT PGA Output Voltage. Connect a 0.1µF capacitor from VOUT to Vss. High impedance when MCS is low. - 4, 16, 2, 32 N.C. Not internally connected. 8 5 ISRC Current-Source Reference. Connect a 50kΩ resistor from ISRC to Vss. 9 6 FSOTCOUT Buffered FSO TC DAC Output. Use a resistor (R _{LIN}) greater than 100kQ, from LINOU 11 8 LINOUT ISRC to correct second order FSO nonlinearity errors. Leave unconnected if nused. 12 9 LINDACEFF Reference Input to FSO Linearity DAC. Output Voltage. Connect 0.1µF capacitor from TDAC to Vss. 14	PIN				
2 29 INM Negative Sensor Input. Input Impedance > 1MΩ. Rail-to-rail Input range. 3 30 AMP+ Positive Input of General-Purpose Operational Amplifier 4 31 AMP- Negative Input of General-Purpose Operational Amplifier 5 1 AMPOUT Output of General-Purpose Operational Amplifier 6 2 BDRIVE Sensor Excitation Current. This pin drives a nominal 0.5mA through the sensor. 7 3 VOUT PCA Output Voitage. Connect a 0.1µF capacitor from VOUT to Vss. High impedance when MCS is low. - 4,16. N.C. Not Internally connected. 8 5 ISRC Current-Source Reference. Connect a 50kΩ resistor from ISRC to Vss. 9 6 FSOTCOUT Buffered FSO Linearity DAC Output. Use a resistor (Ru) greater than 100kΩ from LINDU 11 8 LINOUT Current-Source Reference Input to FSO Innelinearity errors. Leave unconnected if not correcting second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity errors. 12 9 LINDAC FFSO Linearity DAC Output Voltage. Connect a 0.1µF capacitor from OTCDAC to Vss. 14 11 Vss Negative Power Supply inpu	SO	TQFP	NAME	FUNCTION	
3 30 AMP+ Positive Input of General-Purpose Operational Amplifier 4 31 AMP Negative Input of General-Purpose Operational Amplifier 5 1 AMPOLT Output of General-Purpose Operational Amplifier 6 2 BRIVE Sensor Excitation Current. This pin drives a nominal 05mA through the sensor. 7 3 VOUT PCA Output Voltage. Connect a 0.1µF capacitor from VOUT to Vss. High Impedance when MCS is low. 4, 16, 22, 32 N.C. Not internally connected. 8 5 ISRC Current Source Reference. Connect a 50kΩ resistor (Rstr 2 ≤ 50kΩ). 10 7 VBBUF Buffered FSO TC DAC Output. The to ISRC with a resistor (Rstr 2 ≤ 50kΩ). 11 8 LINOUT ISRC to correct second order FSO nonlinearity prorts. Leave unconnected if unused. 11 8 LINDACREF Reference Input to FSO Linearity DAC. Nomelty To Lave prost. Leave unconnected if not correcting second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO Innearity DAC. Nomelty term OTCDAC to Vss. 14 11 Vss Negative Power Supply Input Not To TSO DAC Coutput Voltage. Connect a 0.1µF capacitor from OTCDAC to Vss.	1	28	INP	Positive Sensor Input. Input impedance >1M Ω . Rail-to-rail input range.	
4 31 AMP Negative Input of General-Purpose Operational Amplifier 5 1 AMPOUT Output of General-Purpose Operational Amplifier. High impedance when MCS is low. 6 2 BDRIVE Sensor Excitation Current. This pin drives a nominal 0.5mA through the sensor. 7 3 VOUT PGA Output Voltage. Connect a 0.1μF capacitor from VOUT to Vss. High impedance when MCS is low. - 4,16. N.C. Not internally connected. 8 5 ISRC Current-Source Reference. Connect a 50k0 resistor from ISRC to Vss. 9 6 FSOTCOUT Buffered FSO Utage (the voltage at BDRIVE). Leave unconnected if unused. 10 7 VBBUF Buffered FSO Linearity DAC Output. Use a resistor (R _{LIN}) greater than 100kΩ, from LINOU to ISRC to correct second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity errors. 12 9 LINDAC FSO Linearity DAC Output Voltage. Connect 0.1µF capacitor from FSODAC to Vss. 14 1 Vss Negative Power Supply Input FSO DAC Output Voltage. Connect a 0.1µF capacitor from FSODAC to Vss. 15 12 OTCDAC FSD DAC Output Voltage. Connect a 0.1µF capacitor from FSODAC to Vss.	2	29	INM	Negative Sensor Input. Input impedance >1M Ω . Rail-to-rail input range.	
5 1 AMPOUT Output of General-Purpose Operational Amplifier. High impedance when MCS is low. 6 2 BDRVE Sensor Excitation Current. This pin drives a nominal 0.5mA through the sensor. 7 3 VOUT MCS is low. PGA Output Voltage. Connect a 0.1µF capacitor from VOUT to Vss. High impedance when MCS is low. - 4,16, 22,32 N.C. Not internally connected. Not internally connected. 8 5 ISRC Current-Source Reference. Connect a 50kΩ resistor from ISRC to Vss. 9 6 FSOTCOUT Buffered FSO TC DAC Output. Tie to ISRC with a resistor (Rstr; ≥ 50kΩ). 10 7 VBBUF Buffered FSO Linearity DAC Output. Use a resistor (Rstr; ≥ 50kΩ). 11 8 LINOUT to ISRC to correct second order FSO nonlinearity errors. 12 9 LINDACEFF Reference input to FSO Linearity DAC. Normally tied to VOUT. 13 10 LINDAC FSO Linearity DAC Output Voltage. Connect a 0.1µF capacitor from TCDAC to Vss. 14 11 Vss Negative Power Supply Input Serial Apput (data from EEPROM), active high. CMOS logic-level input pin through which th MAX1457 is internal registers are updated with EEPROM corresincerince input w	3	30	AMP+	Positive Input of General-Purpose Operational Amplifier	
6 2 BDRIVE Sensor Excitation Current. This pin drives a nominal 0.5mA through the sensor. 7 3 VOUT PGA Output Voltage. Connect a 0.1µF capacitor from VOUT to Vss. High impedance when MCS is low. - 4, 16, 22, 32 N.C. Not internally connected. 8 5 ISRC Current-Source Reference. Connect a 50kp resistor from ISRC to Vss. 9 6 FSOTCOUT Buffered FSO TC DAC Output. Tie to ISRC with a resistor (Rsr; 2 50kp). 10 7 VBBUF Buffered FSO Linearity DAC Output. Use a resistor (Rsr; 0 greater than 100kp2, from LINOU to ISRC to correct SO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity persons. 11 8 LINDACREF Reference Input to FSO Linearity DAC. Normality errors. 12 9 LINDACREF Reference Input to FSO Linearity DAC. Normality errors. 13 10 LINDAC FSO DAC OFFSET TO AC Output Voltage. Connect a 0.1µF capacitor from TSODAC to Vss. 14 11 Vss Negative Power Supply Input 0.1µF capacitor from FSOTAC to Vss. 15 12 OTCDAC OFFSET TO AC Output Voltage. Connect a 0.1µF capacitor from FSOTAC to Vss. 17	4	31	AMP-	Negative Input of General-Purpose Operational Amplifier	
7 3 VOUT PGA Output Voltage. Connect a 0.1µF capacitor from VOUT to Vss. High Impedance when MCS is low. - 4,16, 22,32 N.C. Not Internally connected. 8 5 ISRC Current-Source Reference. Connect a 50kΩ resistor from ISRC to Vss. 9 6 FSOTCOUT Buffered FSO TC DAC Output. Tie to ISRC with a resistor (Rst_2 > 50kΩ). 10 7 VBBUF Buffered FSO Linearity DAC Output. Use a resistor (Rt_n) greater than 100kΩ, from LINOU to ISRC to correct second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity errors. 12 9 LINDACREF Reference Input to FSO Linearity DAC. Normally tied to VOUT. 13 10 LINDAC FSO Linearity DAC Output Voltage. Connect a 0.1µF capacitor from OTCDAC to Vss. 14 11 Vs Negative Power Supply Input Second order FSO DAC output Voltage. Connect a 0.1µF capacitor from FSOTCDAC to Vss. 17 14 FSOTCAC FSO TC DAC Output Voltage. Connect a 0.1µF capacitor from FSOTCAC to Vss. 18 15 OFSTDAC OFFSET DAC Output Voltage. Connect a 0.1µF capacitor from FSOTCAC to Vss. 19 17 EDO MAX1457's Internal TegIsters are updated with EEPROM. Coefficient	5	1	AMPOUT	Output of General-Purpose Operational Amplifier. High impedance when MCS is low.	
7 3 VOI1 MCS is low. 4, 16, 22, 32 N.C. Not internally connected. 8 5 ISRC Current-Source Reference. Connect a 50kΩ resistor from ISRC to Vss. 9 6 FSOTCOUT Buffered FSO TC DAC Output. The to ISRC with a resistor (Rstrc ≥ 50kΩ). 10 7 VBBUF Buffered FSO TC DAC Output. The to ISRC with a resistor (Rstrc ≥ 50kΩ). 11 8 LINOUT to ISRC to correct second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity errors. 12 9 LINDACE Reference Input to FSO Linearity DAC. Normally tiled to VOUT. 13 10 LINDAC FSO Encentry DAC Output Voltage. Connect a 0.1µF capacitor from OTDAC to Vss. 14 11 Vss Negative Power Supply Input FSO TC DAC OFFSET TC DAC Output Voltage. Connect a 0.1µF capacitor from OTDAC to Vss. 16 13 FSODAC FSO TC DAC Output Voltage. Connect a 0.1µF capacitor from SDAC to Vss. 17 14 FSOTCDAC FSO TC DAC Output Voltage. Connect a 0.1µF capacitor from OTEDAC to Vss. 19 17 EDO Serial Input (data from EEPROM), active high. CMOS logic-level input which the MAX1457 is internal registers are updated with EEPROM. Temperature-compensati	6	2	BDRIVE	Sensor Excitation Current. This pin drives a nominal 0.5mA through the sensor.	
- 22, 32 N.C. Not internally connected. 8 5 ISRC Current-Source Reference. Connect a 50kΩ resistor from ISRC to Vss. 9 6 FSOTCOUT Buffered FSO TC DAC Output. Tie to ISRC with a resistor (Rstc ≥ 50kΩ). 10 7 VBBUF Buffered FSO TC DAC Output. Tie to ISRC with a resistor (Rtnc) ≥ 50kΩ. 11 8 LINOUT Istfered FSO Linearity DAC Output. Use a resistor (Rtnc) greater than 100kΩ, from LINOU to ISRC to correct second order FSO nonlinearity errors. Leave unconnected If not correcting second order FSO nonlinearity errors. Leave unconnected If not correcting second order FSO nonlinearity errors. 12 9 LINDACREF Reference Input to FSO Linearity DAC. Normally tied to VOUT. 13 10 LINDAC FSO Linearity DAC Output Voltage. Connect a 0.1µF capacitor from OTCDAC to Vss. 14 11 Vss Negative Power Supply Input 15 12 OTCDAC OFFSET TC DAC Output Voltage. Connect a 0.1µF capacitor from FSOTCDAC to Vss. 17 14 FSOTCDAC FSO TCDAC Output Voltage. Connect a 0.1µF capacitor from FSDTAC to Vss. 18 15 OFFSET DAC Output Voltage. Connect a 0.1µF capacitor from FSDTAC to Vss. 19 17	7	3	VOUT	PGA Output Voltage. Connect a $0.1\mu\text{F}$ capacitor from VOUT to Vss. High impedance when MCS is low.	
9 6 FSOTCOUT Buffered FSO TC DAC Output. Tie to ISRC with a resistor (Rstc ≥ 50kΩ). 10 7 VBBUF Buffered Bridge Voltage (the voltage at BDRIVE). Leave unconnected if unused. 11 8 LINOUT Buffered FSO Linearity DAC Output. Use a resistor (Rstr), greater than 100kΩ, from LINOU to ISRC to correct second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity errors. 12 9 LINDACREF Reference Input to FSO Linearity DAC. Normally tied to VOUT. 13 10 LINDAC FSO Linearity DAC Output Voltage. Connect 0.1µF capacitor from LINDAC to Vss. 14 11 Vss Negative Power Supply Input 15 12 OTCDAC OFFSET TC DAC Output Voltage. Connect a 0.1µF capacitor from FSOTCDAC to Vss. 18 15 OFSTDAC OFFSET DAC Output Voltage. Connect a 0.1µF capacitor from FSOTDAC to Vss. 19 17 EDO Serial Input (data from EEPROM), active high. CMOS logic-level input pin through which the MAX1457 gives external commands to the EEPROM. Temperature-compensation data is available through this pin. Becomes high Impedance when MCS is low. 21 19 ECLK CMOS Logic-Level Clock Output for external EEPROM. CMOS logic-level output pin through which the MAX1457 givse external EEPROM. CMOS logic-	_		N.C.	Not internally connected.	
10 7 VBBUF Buffered Bridge Voltage (the voltage at BDRIVE). Leave unconnected if unused. 11 8 LINOUT Buffered FSO Linearity DAC Output. Use a resistor (R _{LIN}) greater than 100kΩ, from LINOU to ISRC to correct second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity errors. 12 9 LINDACREF Reference Input to FSO Linearity DAC. Normally tied to VOUT. 13 10 LINDAC FSO Linearity DAC. Output Voltage. Connect 0.1µF capacitor from LINDAC to Vss. 14 11 Vss Negative Power Supply Input 15 12 OTCDAC OFFSET TC DAC Output Voltage. Connect a 0.1µF capacitor from OTCDAC to Vss. 16 13 FSODAC FSO DAC Output Voltage. Connect a 0.1µF capacitor from FSOTCDAC to Vss. 17 14 FSOTCDAC OFFSET DAC Output Voltage. Connect a 0.1µF capacitor from OFSTDAC to Vss. 18 15 OFFSET DAC Output Voltage. Connect a 0.1µF capacitor from OFSTDAC to Vss. 20 18 EDI Serial Input (data to EEPROM), active high. CMOS logic-level output pin through which the MAX1457 gives external commands to the EEPROM. Temperature-compensation data is available through this pin. Becomes high impedance when MCS is low. <td>8</td> <td>5</td> <td>ISRC</td> <td>Current-Source Reference. Connect a 50kΩ resistor from ISRC to V_{SS}.</td>	8	5	ISRC	Current-Source Reference. Connect a 50k Ω resistor from ISRC to V _{SS} .	
11 8 LINOUT Buffered FSO Linearity DAC Output. Use a resistor (RLIN) greater than 100kΩ, from LINOU to ISRC to correct second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity errors. 12 9 LINDACREF Reference Input to FSO Linearity DAC. Normally tied to VOUT. 13 10 LINDAC FSO Linearity DAC Output Voltage. Connect 0.1µF capacitor from LINDAC to Vss. 14 11 Vss Negative Power Supply Input 15 12 OTCDAC OFFSET TC DAC Output Voltage. Connect a 0.1µF capacitor from OTCDAC to Vss. 16 13 FSODAC FSO LaC Output Voltage. Connect a 0.1µF capacitor from FSOTCAC to Vss. 17 14 FSOTCAC FSO TC DAC Output Voltage. Connect a 0.1µF capacitor from OFSDAC to Vss. 18 15 OFSTDAC OFFSET DAC Output Voltage. Connect a 0.1µF capacitor from OFSDAC to Vss. 20 18 EDI Serial Input (data to EPROM), active high. CMOS logic-level input pin through which the MAX1457's internal registers are updated with EEPROM. Temperature-compensation data is available through this pin. Becomes high impedance when MCS is low. 21 19 ECLK CMOS Logic-Level Clock Output for external EPROM. Temperature-compe	9	6	FSOTCOUT	Buffered FSO TC DAC Output. Tie to ISRC with a resistor ($R_{STC} \ge 50 k\Omega$).	
118LINOUTto ISRC to correct second order FSO nonlinearity errors. Leave unconnected if not correcting second order FSO nonlinearity perrors.129LINDACREFReference Input to FSO Linearity DAC. Normally tied to VOUT.1310LINDACFSO Linearity DAC Output Voltage. Connect 0.1µF capacitor from LINDAC to Vss.1411VssNegative Power Supply Input1512OTCDACOFFSET TC DAC Output Voltage. Connect a 0.1µF capacitor from OTCDAC to Vss.1613FSODACFSO TAC Output Voltage. Connect a 0.1µF capacitor from FSOTAC to Vss.1714FSOTCDACFSO TC DAC Output Voltage. Connect a 0.1µF capacitor from OFSTDAC to Vss.1815OFSTDACOFFSET DAC Output Voltage. Connect a 0.1µF capacitor from OFSTDAC to Vss.1917EDOSerial Input (data from EEPROM), active high. CMOS logic-level input pin through which the MAX1457 is internal registers are updated with EEPROM coefficients. Disabled when MCS i low.2018EDISerial Output (data to EEPROM), active high. CMOS logic-level output pin through which the MAX1457 gives external commands to the EEPROM. Temperature-compensation data is available through this pin. Becomes high impedance when MCS is low.2119ECLKCMOS Logic-Level Clock Output for external EEPROM. High impedance when MCS is low.2321FOUTFrequency Adjust. Connect to Vss with a 1.5MΩ resistor (Rosc) to set internal oscillator fre query to 100kHz. Connect to Vsp.2423FADJMaster Chip Select. The MAX1457 is selected when MCS is high. Leave unconnected for normal operation (10	7	VBBUF	Buffered Bridge Voltage (the voltage at BDRIVE). Leave unconnected if unused.	
1310LINDACFSO Linearity DAC Output Voltage. Connect 0.1µF capacitor from LINDAC to Vss.1411VssNegative Power Supply Input1512OTCDACOFFSET TC DAC Output Voltage. Connect a 0.1µF capacitor from OTCDAC to Vss.1613FSODACFSO DAC Output Voltage. Connect a 0.1µF capacitor from FSODAC to Vss.1714FSOTCDACFSO TC DAC Output Voltage. Connect a 0.1µF capacitor from FSOTCDAC to Vss.1815OFSTDACOFFSET DAC Output Voltage. Connect a 0.1µF capacitor from OFSTDAC to Vss.1917EDOSerial Input (data from EEPROM), active high. CMOS logic-level input pin through which the MAX1457's internal registers are updated with EEPROM coefficients. Disabled when MCS I low.2018EDISerial Output (data to EEPROM), active high. CMOS logic-level output pin through which the MAX1457 gives external commands to the EEPROM. Temperature-compensation data is available through this pin. Becomes high impedance when MCS is low.2119ECLKCMOS Logic-Level Clock Output for external EEPROM. High impedance when MCS is low.2220ECSChip-Select Output for external EEPROM operation. High impedance when MCS is low.2321FOUTFrequency Output. Internal oscillator output signal. Normally left open.2423FADJFrequency Adjust. Connect to Vss with a 1.5MΩ resistor (Rosc) to set internal oscillator fre quency to 100kHz. Connect to VDp with a 400kΩ resistor (RBIAS). Connect a 0.1µF bypass capacitor from NBIAS to Vss.2625NBIASBias Setting Pin. Connect to Vpp with a 400kΩ resistor (RBIAS). Co	11	8	LINOUT		
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2423FADJFrequency Adjust. Connect to VSS with a 1.5MΩ resistor (RoSc) to set internal oscillator fre quency to 100kHz. Connect a 0.1µF bypass capacitor from FADJ to VSS.2524MCSMaster Chip Select. The MAX1457 is selected when MCS is high. Leave unconnected for normal operation (internally pulled up to VDD with 1MΩ resistor). External 5kΩ pull-up may be required in noisy environments.2625NBIASBias Setting Pin. Connect to VDD with a 400kΩ resistor (RBIAS). Connect a 0.1µF bypass capacitor from NBIAS to VSS.2726AGNDMid-Supply Reference for Analog Circuitry. Connect a 0.1µF capacitor from VSS to AGND.	22	20	ECS		
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26 25 NBIAS capacitor from NBIAS to V _{SS} . 27 26 AGND Mid-Supply Reference for Analog Circuitry. Connect a 0.1µF capacitor from V _{SS} to AGND.	25	24	MCS	normal operation (internally pulled up to V _{DD} with 1M Ω resistor). External 5k Ω pull-up may	
	26	25	NBIAS	Bias Setting Pin. Connect to V _{DD} with a 400k Ω resistor (R _{BIAS}). Connect a 0.1µF bypass	
28 27 V _{DD} Positive Power-Supply Input. Connect a 0.1µF capacitor from V _{DD} to V _{SS} .	27	26	AGND	Mid-Supply Reference for Analog Circuitry. Connect a 0.1µF capacitor from V _{SS} to AGND.	
	28	27	V _{DD}	Positive Power-Supply Input. Connect a $0.1\mu F$ capacitor from V_{DD} to V_{SS} .	

_Detailed Description

The MAX1457 provides an analog amplification path for the sensor signal and a digital path for calibration and temperature correction. Calibration and correction are achieved by varying the offset and gain of a programmable-gain amplifier (PGA) and by varying the sensor bridge current. The PGA utilizes a switched-capacitor CMOS technology, with an input-referred offset trimming range of ± 100 mV (20mV/V) and an approximate 3µV (input referred, at minimum gain of 54V/V) resolution (16 bits). The PGA provides eight gain values from 54V/V to 306V/V. The bridge current source is programmable from 0.1mA to 2mA, with a 15nA step size.

The MAX1457 uses five 16-bit DACs with calibration coefficients stored in a low-cost external EEPROM. This memory (an external 4096-bit EEPROM) contains the following calibration coefficients as 16-bit words:

- FSO (full-span output)
- FSO TC (including nonlinearities)
- Offset
- Offset TC (including nonlinearities)
- Pressure nonlinearity

Figure 1 shows a typical pressure-sensor output and defines the offset, full-scale, and full-span output values as a function of voltage.

Offset Correction

MAX1457

Initial offset calibration is accomplished by reading a 16-bit word (coefficient) from the EEPROM and writing it to the OFFSET DAC. The resulting voltage (OFSTDAC) is fed into a summing junction at the PGA output for compensating the sensor offset with a resolution of ± 0.2 mV ($\pm 0.005\%$ FSO).

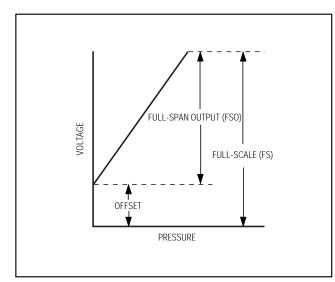


Figure 1. Typical Pressure-Sensor Output

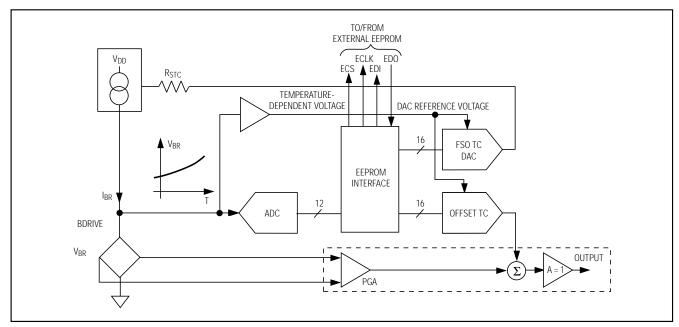


Figure 2. Simplified Diagram of Temperature Error Correction



FSO Calibration

Two adjustments are required for FSO calibration. First set the coarse gain by digitally selecting the PGA gain. Then calibrate the bridge current by writing a 16-bit calibration coefficient word to the FSO DAC. These two adjustments result in a calibration resolution of ± 0.2 mV ($\pm 0.005\%$ FSO).

Linear Temperature Compensation

Temperature errors are compensated by writing 16-bit calibration coefficients into the OFFSET TC DAC and the FSO TC DAC (changing the current-source value through resistive feedback from the FSOTCDAC pin to the ISRC pin). The piezoresistive sensor is powered by a current source resulting in a temperature-dependent bridge voltage. The reference inputs of the OFFSET TC DAC and FSO TC DAC are connected to the bridge voltage. For a fixed digital word, the DAC output voltages track the bridge voltage as it varies with temperature (quasi-linearly).

Multislope Temperature Compensation

The MAX1457 utilizes multislope temperature compensation, allowing for compensation of arbitrary error curves restricted only by the available adjustment range and the shape of the temperature signal.

The MAX1457 offers a maximum of 120 calibration points (each consisting of one OFFSET TC coefficient and one FSO TC coefficient) over the operating temperature range. Each 16-bit calibration coefficient provides compensation of the output (either offset or FSO) with $\pm 0.2mV$ (0.005% FSO) resolution. A 12-bit ADC measures the temperature-dependent bridge voltage (BDRIVE) and selects (by addressing the EEPROM) the corresponding offset and FSO calibration data within a specific narrow temperature span (e.g., $\cong 1^{\circ}$ C). The 120-segment compensation enables the MAX1457 to compensate temperature errors for a broad range of sensors (Figure 2).

Calculate the correction coefficients by curve-fitting to sensor-error test data. More test points allow for better curve-fit accuracy but result in increased test overhead. The remaining error is further affected by the slope of the temperature errors. For example, correcting a 6% nonlinearity over temperature with 60 segments (half of the available calibration points) with perfect curve fitting yields an error on the order of 0.1% (6%/60). Figure 3 illustrates this compensation.

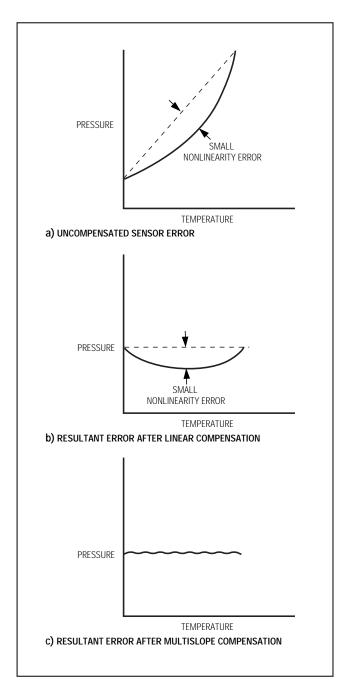


Figure 3. Multislope Temperature Compensation

Pressure Nonlinearity Correction

The MAX1457 corrects pressure nonlinearity in an analog fashion by providing a resistive feedback path (resistor R_{LIN} in Figure 4) from a buffered main output (LINOUT pin) to the current source (ISRC pin). The feedback coefficient is then set by writing a 16-bit word to the FSO LIN DAC.

For many silicon sensors, this type of nonlinearity correction may reduce sensor nonlinearity by an order of magnitude.

_Applications Information

Ratiometric Output Configuration

Ratiometric output configuration provides an output that is proportional to the power-supply voltage. When used with ratiometric ADCs, this output provides digital pressure values independent of supply voltage.

The MAX1457 has been designed to provide a highperformance ratiometric output with a minimum number of external components (Figure 5). These external components typically include an external EEPROM (93C66), decoupling capacitors, and resistors.

2-Wire, 4-20mA Configuration

In this configuration, a 4mA current is used to power a transducer, and an incremental current of 0 to 16mA proportional to the measured pressure is transmitted over the same pair of wires. Current output enables long-distance transmission without a loss of accuracy due to cable resistance.

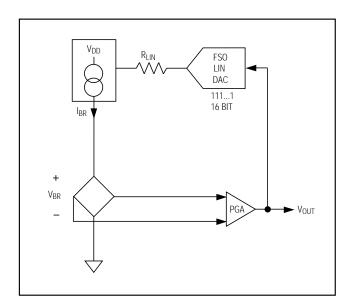


Figure 4. Pressure Nonlinearity Correction



Only a few components (Figure 6) are required to build a 4–20mA output configuration. A low-quiescent-current voltage regulator with a built-in bandgap reference (such as the REF02) should be used. Since the MAX1457 performs temperature and gain compensation of the circuit, the temperature stability and calibration accuracy of the reference voltage is of secondary importance.

The external transistor forms the controllable current loop. The MAX1457 controls the voltage across resistor R_A. With R_A = 50Ω , a 0.2V to 1.0V range would be required during the calibration procedure. If needed, the PGA output can be divided using resistors R_B and R_C.

For overvoltage protection, place a Zener diode across $V_{IN^{\rm -}}$ and $V_{IN^{\rm +}}$ (Figure 6). A feedthrough capacitor across the inputs reduces EMI/RFI.

Test System Configuration

The MAX1457 is designed to support an automated production pressure-temperature test system with integrated calibration and temperature compensation. Figure 7 shows the implementation concept for a low-cost test system capable of testing up to five transducer modules connected in parallel. Three-state outputs on the MAX1457 allow for parallel connection of transducers.

The test system shown in Figure 7 includes a dedicated test bus consisting of six wires (the capacitive loading of each transducer module should not exceed the EEPROM fan-out specifications):

- Two power-supply lines
- One analog output voltage line from the transducers to a system digital voltmeter
- Three MicroWire/SPI interface lines: EDI (data-in), EDO (data-out), and ECLK (clock)

For simultaneous testing of more than five transducer modules, use buffers to prevent overloading the data bus.

A digital multiplexer controls the two chip-select signals for each transducer:

- Module Select (MCS) places the selected module into an active state, enabling operation and compensation
- EEPROM Select (ECS) enables writing to the transducer's EEPROM

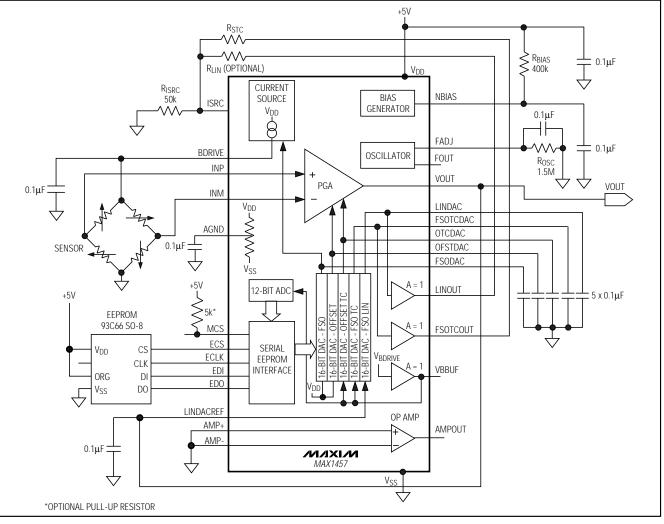


Figure 5. Basic Ratiometric Output Configuration

Sensor Compensation Overview

Compensation requires an examination of the sensor performance over the operating pressure and temperature range. Use two test pressures (e.g., zero and fullspan) and two temperatures. More test pressures and temperatures will result in greater accuracy. A simple compensation procedure can be summarized as follows:

Set reference temperature (e.g., +25°C):

- Initialize each transducer by loading its EEPROM with default coefficients (e.g., based on mean values of offset, FSO, and bridge resistance) to prevent gross overload of the MAX1457.
- Set the initial bridge voltage (with the FSO DAC) to half the supply voltage. The bridge voltage can be

measured by the MAX1457 and returned to the test computer via the serial interface or by using the system digital voltmeter to measure the voltage on either BDRIVE or VBBUF.

- 3) Calibrate the transducer's output offset and FSO using the OFFSET and FSO DACs, respectively.
- 4) Store calibration data in the test computer.

Set next test temperature:

- 5) Calibrate offset and FSO using the OFFSET TC and FSO TC DACs, respectively.
- 6) Store calibration data in the test computer.

Repeat steps 5 and 6 for each required test temperature.

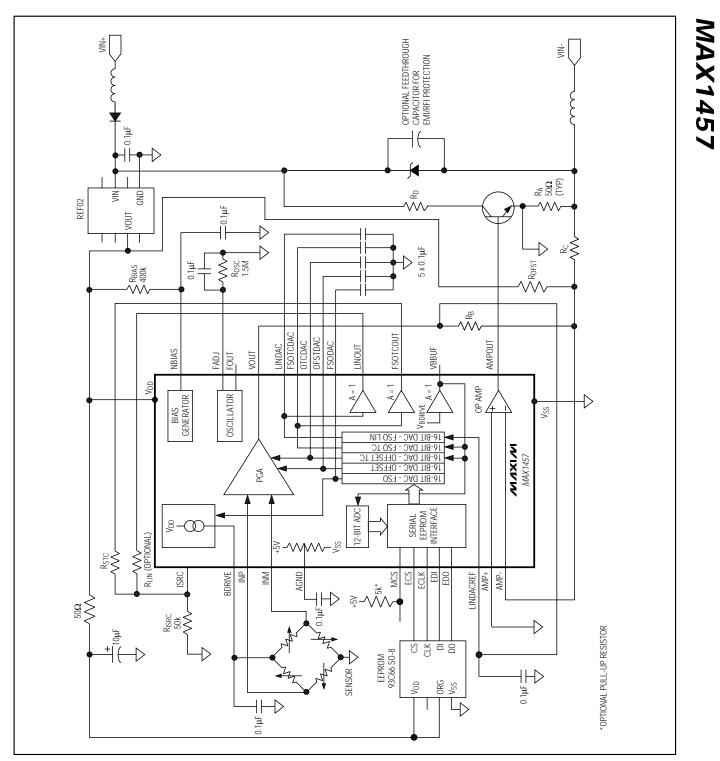


Figure 6. Basic 2-Wire 4–20mA Configuration



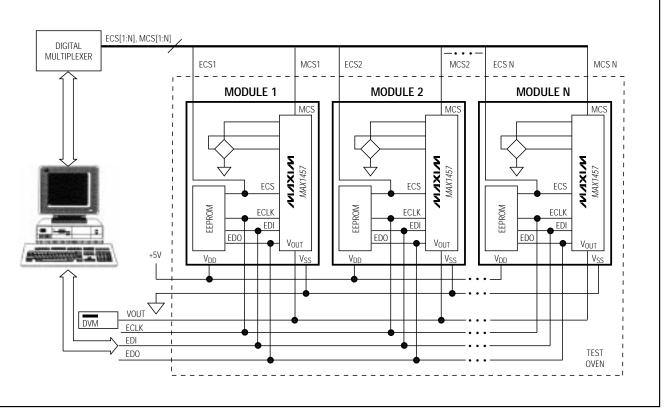


Figure 7. Automated Test System Concept

- 7) Perform curve-fitting to test data.
- 8) Based on a curve-fit algorithm, calculate up to 120 sets of offset and FSO correcting values.
- 9) Download correction coefficients to transducer EEPROM.

10) Perform a final test.

The resulting transducer temperature errors are limited by the following factors:

- Number of selected segments for compensation (up to 120).
- Accuracy of the curve fitting, which depends on the algorithm used, the number of test temperatures, and the sensor temperature error's shape.
- Repeatability of the sensor performance. This will limit the MAX1457's accuracy.

Sensor Calibration and Compensation Example

Calibration and compensation requirements for a sensor involve conversion of the sensor-specific performance into a normalized output curve. An example of the MAX1457's capabilities is shown in Table 1.

As shown in Table 1, a repeatable piezoresistive sensor with an initial offset of 16.4mV and FSO of 55.8mV was converted into a compensated transducer (utilizing the piezoresistive sensor with the MAX1457) with an offset of 0.500V and a span of 4.000V. Nonlinear sensor offset and FSO temperature errors, which were on the order of 4% to 5% FSO, were reduced to under $\pm 0.1\%$ FSO. The graphs in Figure 8 show the output of the uncompensated sensor and the output of the compensated transducer.



Table 1. MAX1457 Sensor Calibration and Compensation

Typical Uncompensated Input (Sensor)
Offset±100% FSO
FSO
Offset TC
Offset TC Nonlinearity
FSO TC
FSO TC Nonlinearity

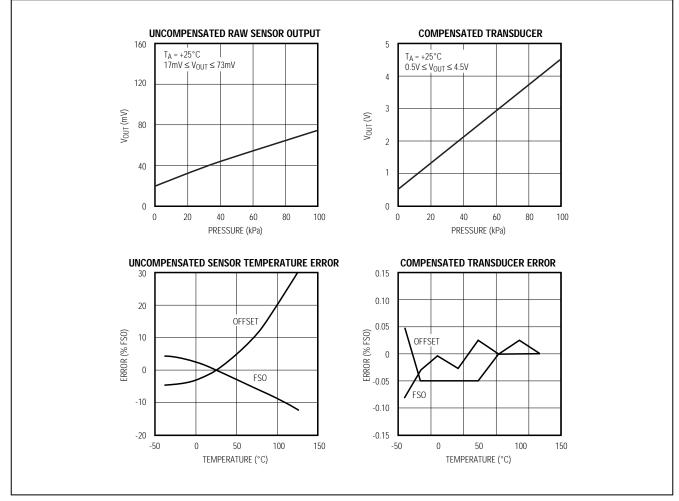


Figure 8. Comparison of an Uncompensated Sensor (left) and a Compensated Transducer (right)

MAX1457 Evaluation ____ Development Kit

To expedite the development of MAX1457-based transducers and test systems, Maxim has produced a MAX1457 evaluation kit (EV kit). First-time users of the MAX1457 are strongly encouraged to use this kit.

The kit is designed to facilitate manual programming of the MAX1457 with a sensor. It includes the following:

- Evaluation board (EV board) with a silicon pressure sensor, ready for customer evaluation.
- Design/applications manual, which describes in detail the architecture and functionality of the MAX1457. This manual was developed for test engineers familiar with data acquisition of sensor data and provides sensor-compensation algorithms and test procedures.
- MAX1457 communication software, which enables programming of the MAX1457 from a computer keyboard (IBM compatible), one module at a time.
- 4) Interface adapter and cable, which allows the connection of the EV board to a PC parallel port.

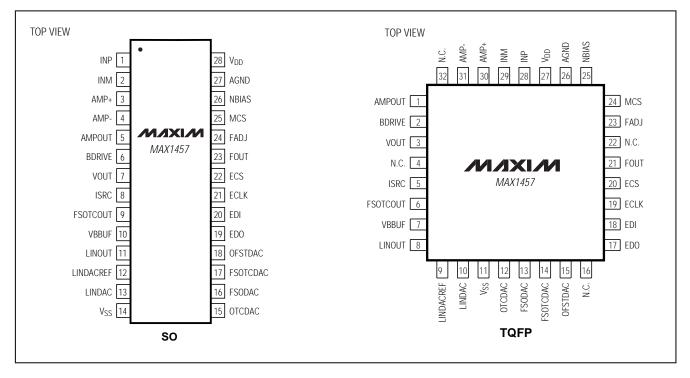
_Chip Information

TRANSISTOR COUNT: 17534 SUBSTRATE CONNECTED TO VSS

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX1457AWI	-40°C to +125°C	28 Wide SO
MAX1457ACJ	-40°C to +125°C	32 TQFP

_Pin Configurations



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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