

M5M5188AP, J-25, -35, -45, -55

65536-BIT(16384-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

This is family of 16384 word by 4-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5188AP, J-25 25 ns (max)
- M5M5188AP, J-35 35 ns (max)
- M5M5188AP, J-45 45 ns (max)
- M5M5188AP, J-55 55 ns (max)
- Low power dissipation Active 300 mW (typ)
- Stand by 5 μ W (typ)
- Power down by \bar{S}
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select (\bar{S}) input

APPLICATION

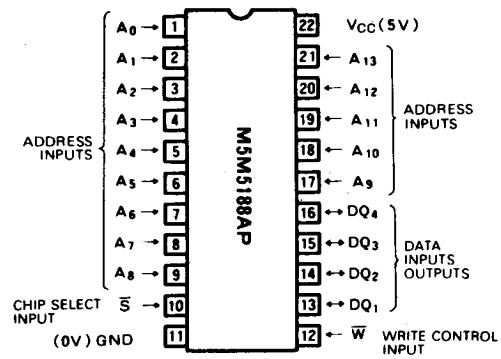
High-speed memory systems

FUNCTION

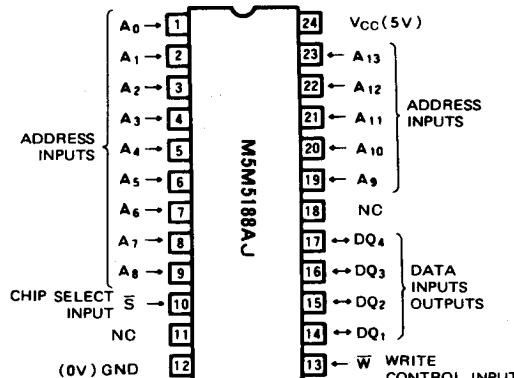
A write operation is executed during the \bar{S} low and \bar{W} low overlap time. In this period, address signals must be stable. When \bar{W} is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting \bar{W} to high, and \bar{S} to low if the address signals are stable, the data is available at the DQ terminal.

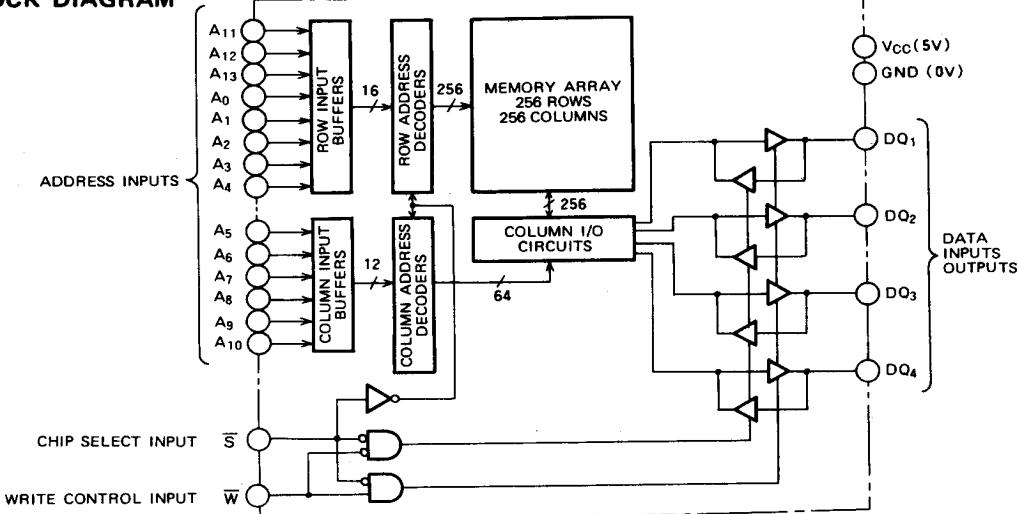
When \bar{S} is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is

PIN CONFIGURATION (TOP VIEW)

Outline 22P4H(DIP)



Outline 24P0J(SOJ) NC: NO CONNECTION

BLOCK DIAGRAM

M5M5188AP, J-25, -35, -45, -55**65536-BIT(16384-WORD BY 4-BIT) CMOS STATIC RAM**

in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal \bar{S} controls the power-down feature. When \bar{S} goes high, power dissipation is reduced extremely. The access time from \bar{S} is equivalent to the address access time.

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|---------------------------|---------------------|---------|------|
| V _{CC} | Supply voltage | With respect to GND | -3.5~7 | V |
| V _I | Input voltage | | -3.5~7 | V |
| V _O | Output voltage | | -3.5~7 | V |
| P _d | Maximum power dissipation | | 1 | W |
| T _{opr} | Operating temperature | | -10~85 | °C |
| T _{stg} | Storage temperature | | -65~150 | °C |

* Pulse width = 20 ns, In case of DC: -0.5V

DC ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|------------------|-------------------------------------|---|--------|-------|----------------------|------|
| | | | Min | Typ | Max | |
| V _{IH} | High-level input voltage | | 2.2 | | V _{CC} +0.3 | V |
| V _{IL} | Low-level input voltage | | -3 * | | 0.8 | V |
| V _{OH} | High-level output voltage | I _{OH} = -4 mA | 2.4 | | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 8 mA | | | 0.4 | V |
| I _I | Input current | V _I = 0 ~ V _{CC} | | | 10 | μA |
| I _{OZ} | Off-state output current | V _I (\bar{S}) = 2.2V, V _O = 0 ~ V _{CC} | | | 10 | μA |
| I _{CC1} | Supply current from V _{CC} | V _I (\bar{S}) = 0.8V Output open | | | 100 | mA |
| I _{CC2} | Stand by current | V _I (\bar{S}) = 2.2V Other V _I ≤ 0.2V | | 15 | 25 | mA |
| I _{CC3} | Stand by current | V _I (\bar{S}) ≥ V _{CC} - 0.2V, Other V _I ≤ 0.2V or V _I ≥ V _{CC} - 0.2V | | 0.001 | 2 | mA |
| C _i | Input capacitance | V _I = GND, V _i = 25mVrms, f = 1MHz | | | 5 | pF |
| C _o | Output capacitance | V _O = GND, V _O = 25mVrms, f = 1MHz | | | 6 | pF |

Note 1. Current flow into an IC is positive, out is negative.

* Pulse width = 20 ns, In case of DC: -0.5V

SWITCHING CHARACTERISTICS (FOR READ CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

| Symbol | Parameter | M5M5188A-25 | | M5M5188A-35 | | M5M5188A-45 | | M5M5188A-55 | | Unit |
|---------------------|--|-------------|-----|-------------|-----|-------------|-----|-------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t _{CR} | Read cycle time | 25 | | 35 | | 45 | | 55 | | ns |
| t _{a(A)} | Address access time | | 25 | | 35 | | 45 | | 55 | ns |
| t _{a(S)} | Chip select access time | | 25 | | 35 | | 45 | | 55 | ns |
| t _{v(A)} | Data valid time after address | 5 | | 5 | | 5 | | 5 | | ns |
| t _{en(S)} | Output enable time after chip selection | 5 | | 5 | | 5 | | 5 | | ns |
| t _{dis(S)} | Output disable time after chip deselection | 0 | 15 | 0 | 15 | 0 | 20 | 0 | 30 | ns |
| t _{pu} | Power-up time after chip selection | 0 | | 0 | | 0 | | 0 | | ns |
| t _{pd} | Power down time after chip deselection | | 25 | | 35 | | 45 | | 55 | ns |

65536-BIT(16384-WORD BY 4-BIT)CMOS STATIC RAM

TIMING REQUIREMENTS (FOR WRITE CYCLE) ($T_a = 0 \sim 70^\circ C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

| Symbol | Parameter | M5M5188A-25 | | M5M5188A-35 | | M5M5188A-45 | | M5M5188A-55 | | Unit |
|----------------------|---|-------------|-----|-------------|-----|-------------|-----|-------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{CW} | Write cycle time | 25 | | 35 | | 45 | | 55 | | ns |
| $t_{SU}(S)$ | Chip select setup time | 20 | | 30 | | 35 | | 40 | | ns |
| $t_{SU}(A)_1$ | Address setup time 1 (\bar{W} CONTROL) | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SU}(A)_2$ | Address setup time 2 (\bar{S} CONTROL) | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{W(W)}$ | Write pulse width | 20 | | 30 | | 35 | | 40 | | ns |
| $t_{REC}(W)$ | Write recovery time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SU}(D)$ | Data setup time | 10 | | 15 | | 20 | | 20 | | ns |
| $t_{H}(D)$ | Data hold time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DIS}(W)$ | Output disable time after \bar{W} low | 0 | 10 | 0 | 15 | 0 | 15 | 0 | 20 | ns |
| $t_{EN}(W)$ | Output enable time after \bar{W} high | 0 | | 0 | | 5 | | 5 | | ns |
| $t_{SU}(A-\bar{W}H)$ | Address to \bar{W} high | 20 | | 30 | | 35 | | 40 | | ns |

CONDITIONS

Input pulse levels 0 to 3V
 Input rise and fall time 5ns
 Input timing reference level 1.5V
 Output timing reference level 0.8V ~ 2V
 Output loads Fig. 1, Fig. 2

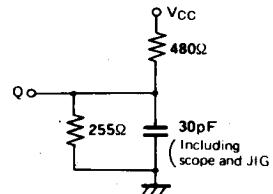


Fig. 1 Output load

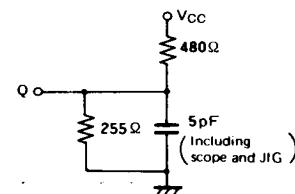
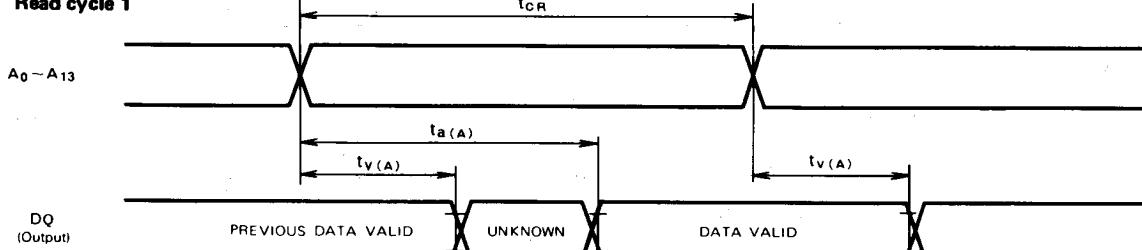


Fig. 2 Output load for t_{EN} , t_{DIS}

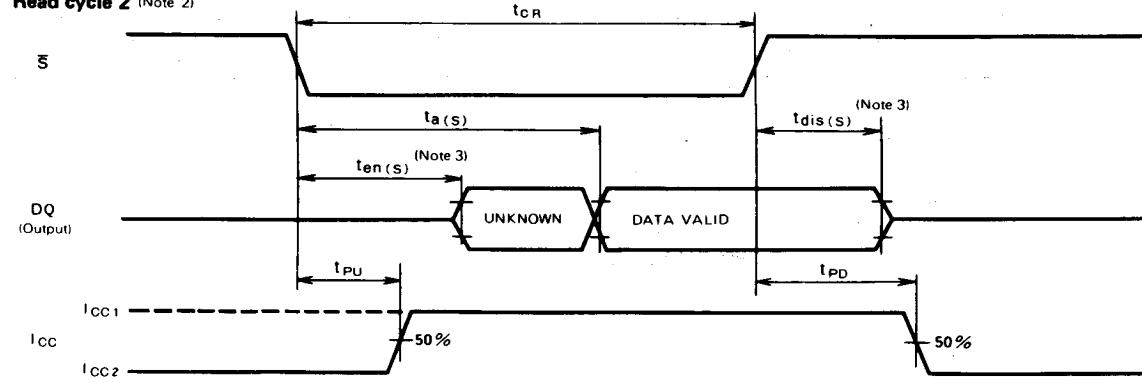
TIMING DIAGRAMS

Read cycle 1



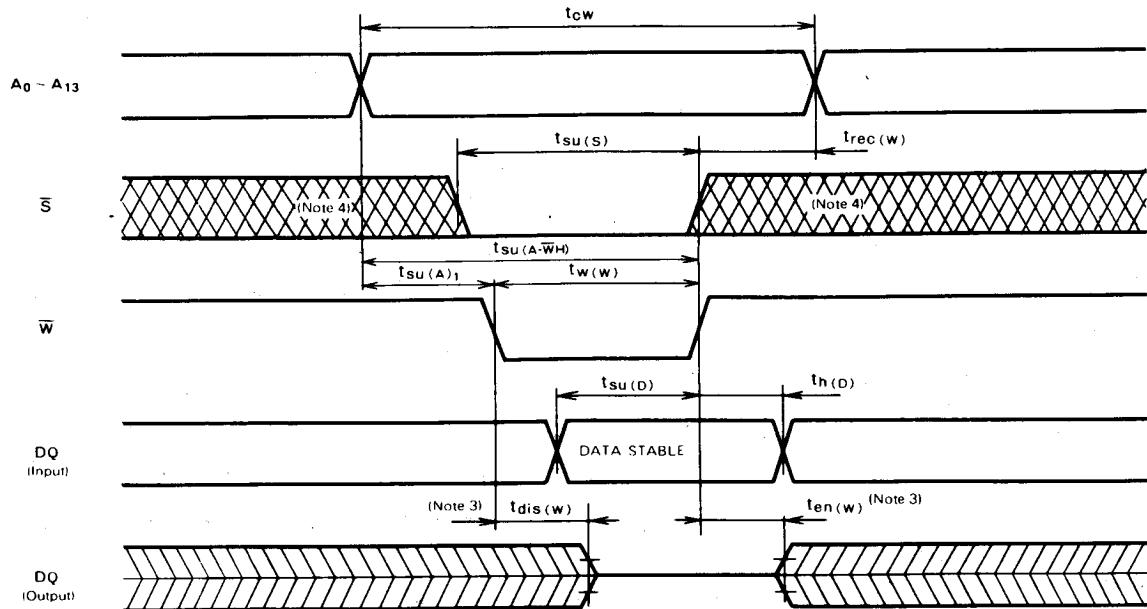
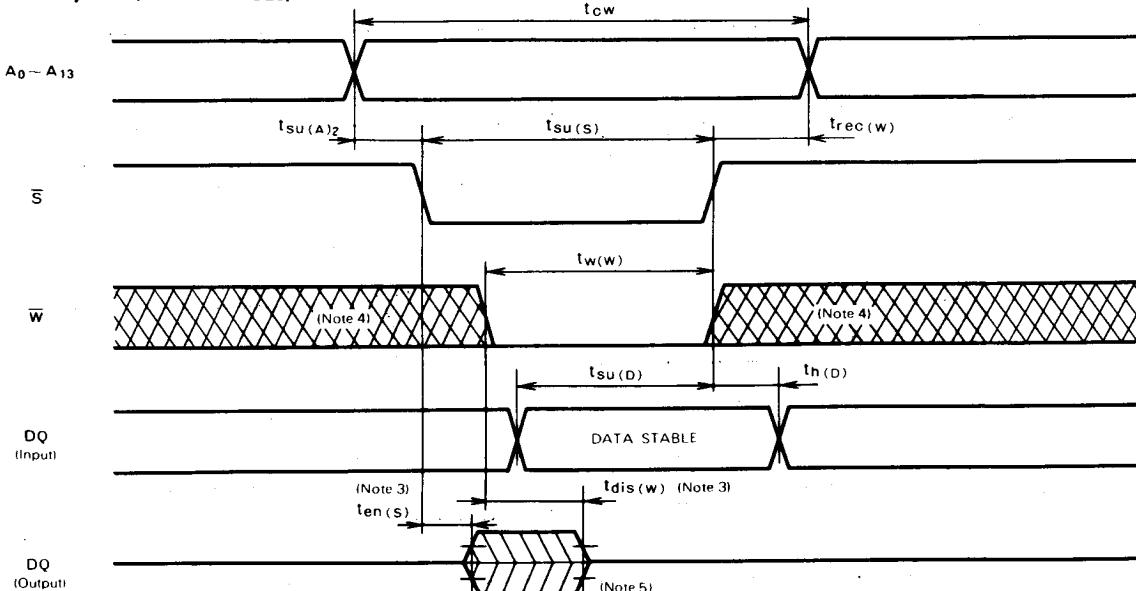
$\bar{W} = H$
 $\bar{S} = L$

Read cycle 2 (Note 2)



Note 2. Addresses valid prior to or coincident with \bar{S} transition low.

3. Transition is measured $\pm 500mV$ from steady state voltage with specified loading in Figure 2.

65536-BIT(16384-WORD BY 4-BIT) CMOS STATIC RAM**TIMING DIAGRAMS****Write cycle 1 (\bar{W} control mode)****Write cycle 2 (\bar{S} control mode)**

Note 4. Hatching indicates the state is don't care.

5. When the falling edge of \bar{W} is simultaneous or prior to the falling edge of \bar{S} , the output is maintained in the high impedance.