Am49LVI28BM

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **31022** Revision **A** Amendment **6** Issue Date **June 17, 2004**

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SUPPLEMENT

Am49LV128BM

Stacked Multi-Chip Package (MCP)
128 Megabit (8 M x 16-Bit) MirrorBit™ Uniform Sector Flash Memory and 32 Mbit (2 M x 16-Bit) pseudo-static RAM with Page Mode

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **Single power supply operation**
  - 3 volt read, erase, and program operations
- **Manufactured on 0.23 µm MirrorBit process technology**
- **SecSi™ (Secured Silicon) Sector region**
  - 128-word sector for permanent, secure identification through an 8-word random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked by the customer
- **Flexible sector architecture**
  - Two hundred fifty-six 32 Kword sectors
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **Minimum 100,000 erase cycle guarantee per sector**
- **20-year data retention at 125°C**

PERFORMANCE CHARACTERISTICS

- **High performance**
  - As fast as 105 ns access time
  - 25 ns page read times
  - 0.5 s typical sector erase time
  - 15 µs typical write buffer word programming time: 16-word write buffer reduces overall programming time for multiple-word updates
  - 4-word page read buffer
  - 16-word write buffer
- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - 30 mA typical active read current
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current
- **Package option**
  - 64-ball FBGA

SOFTWARE & HARDWARE FEATURES

- **Software features**
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - Unlock Bypass Program command reduces overall multiple-word or byte programming time
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- **Hardware features**
  - Sector Group Protection: hardware-level method of preventing write operations within a sector group
  - Temporary Sector Group Unprotect: V_{ID}-level method of changing code in locked sector groups
  - WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects last sector regardless of sector protection settings
  - Hardware reset input (RESET#) resets device

PSRAM FEATURES

- **Asynchronous SRAM Interface**
- **Fast Access Time**
  - $t_{CE} = t_{AA}$ = 65 ns max
- **Low Voltage Operating Condition**
  - V_{DD} = 2.7 to + 3.1 V
- **Byte Control by LB# and UB#**

Publication Number: **31022_00** Rev: **A**
Amendment:**6**

GENERAL DESCRIPTION

The 128 Mbit MirrorBit device is a 128 Mbit, 3.0 volt single power supply flash memory devices organized as 8,388,608 words. The device has a 16-bit wide data bus. The device can be programmed either in the host system or in standard EPROM programmers.

An access time of 105 or 110 ns is available. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0 volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (**WP#/**ACC)** input provides shorter programming times through increased current. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector group to read or program any other sector group and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector group to read any other sector group and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **SecSi™ (Secured Silicon) Sector** provides a 128-word area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

The **Write Protect (WP#**/ACC**)** feature protects the last sector by asserting a logic low on the WP# pin.

AMD MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

RELATED DOCUMENTS

For a comprehensive information on MirrorBit products, including migration information, data sheets, application notes, and software drivers, please see www.amd.com→Flash Memory→Product Information→MirrorBit→Flash Information→Technical Documentation. The following is a partial list of documents closely related to this product:

MirrorBit™ Flash Memory Write Buffer Programming and Page Buffer Read

Implementing a Common Layout for AMD MirrorBit and Intel StrataFlash Memory Devices

Migrating from Single-byte to Three-byte Device IDs

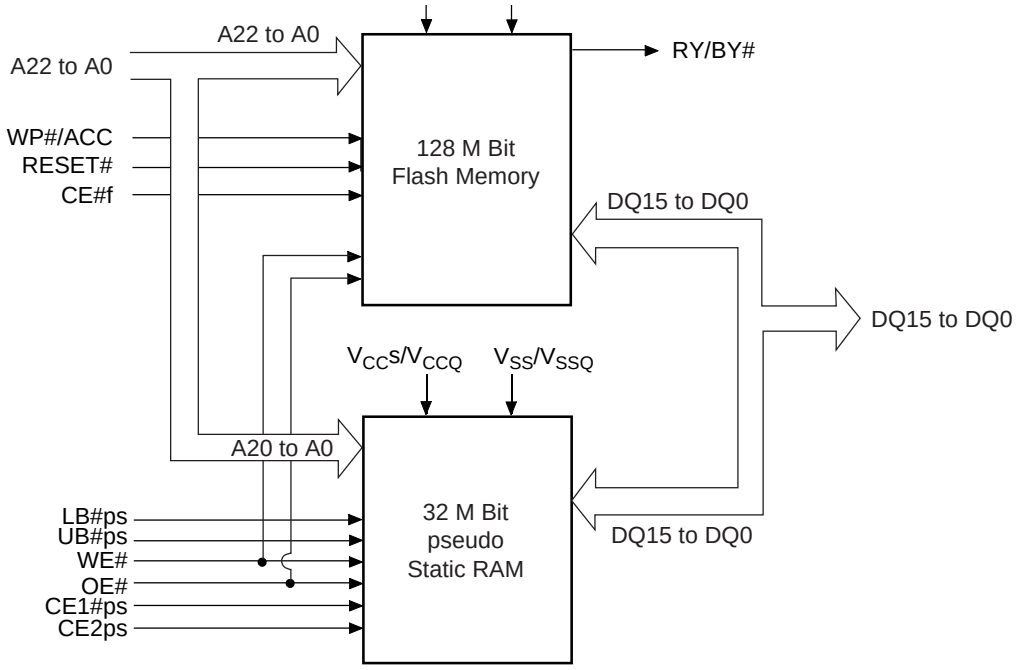
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

Part Number		Am49LV128BM		
Speed/ Voltage Option	Full Voltage Range V_{CC} = 2.7–3.1 V	Flash		pSRAM
		15	11	15, 11
Max. Access Time (ns)		105	110	65
Max. CE# Access Time (ns)		105	110	65
Max. Page access time (t_{PACC})		25	30	20
Max. OE# Access Time (ns)		25	30	20

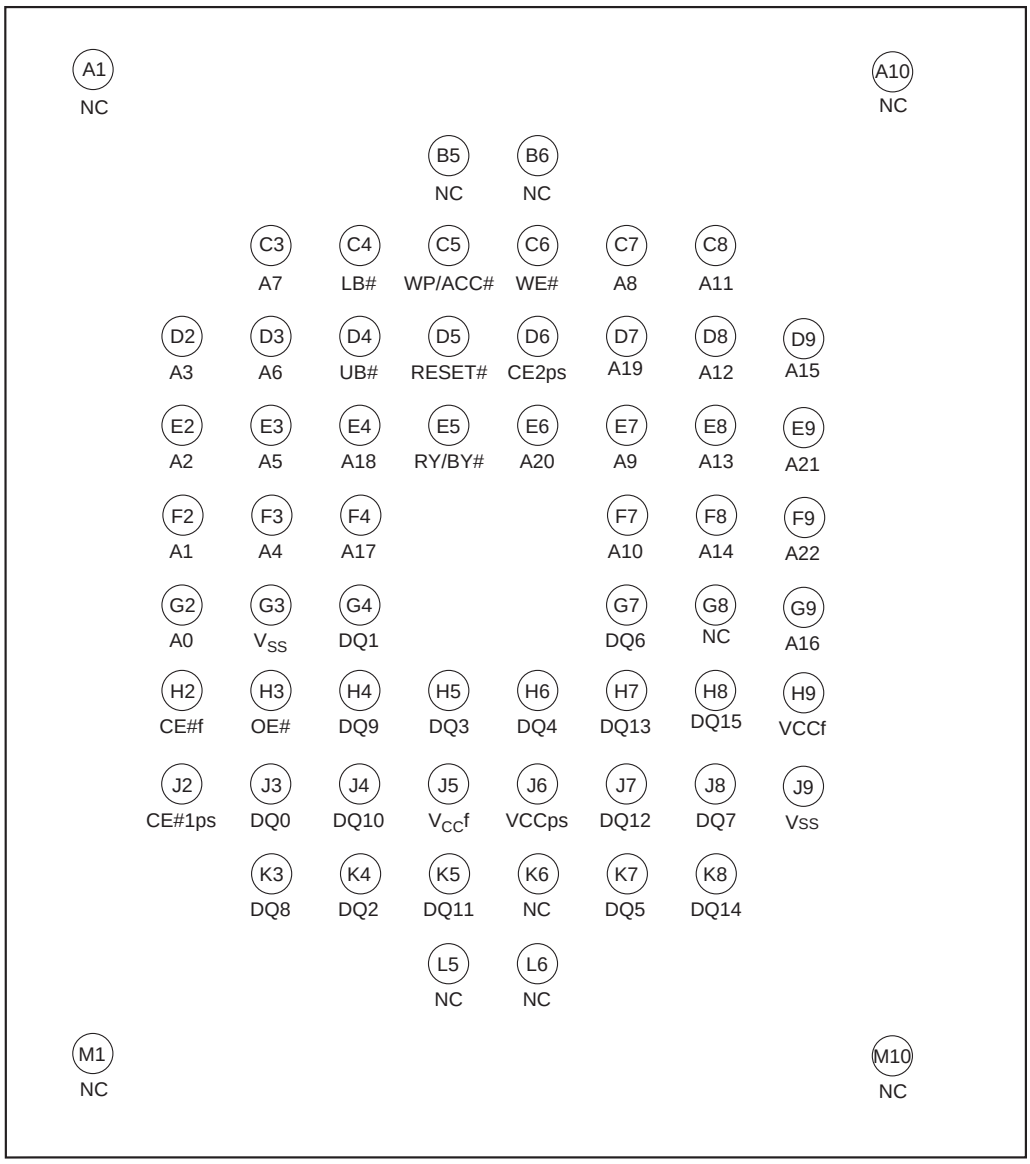
Notes:
1. See "AC Characteristics" for full specifications.

MCP BLOCK DIAGRAM



CONNECTION DIAGRAMS

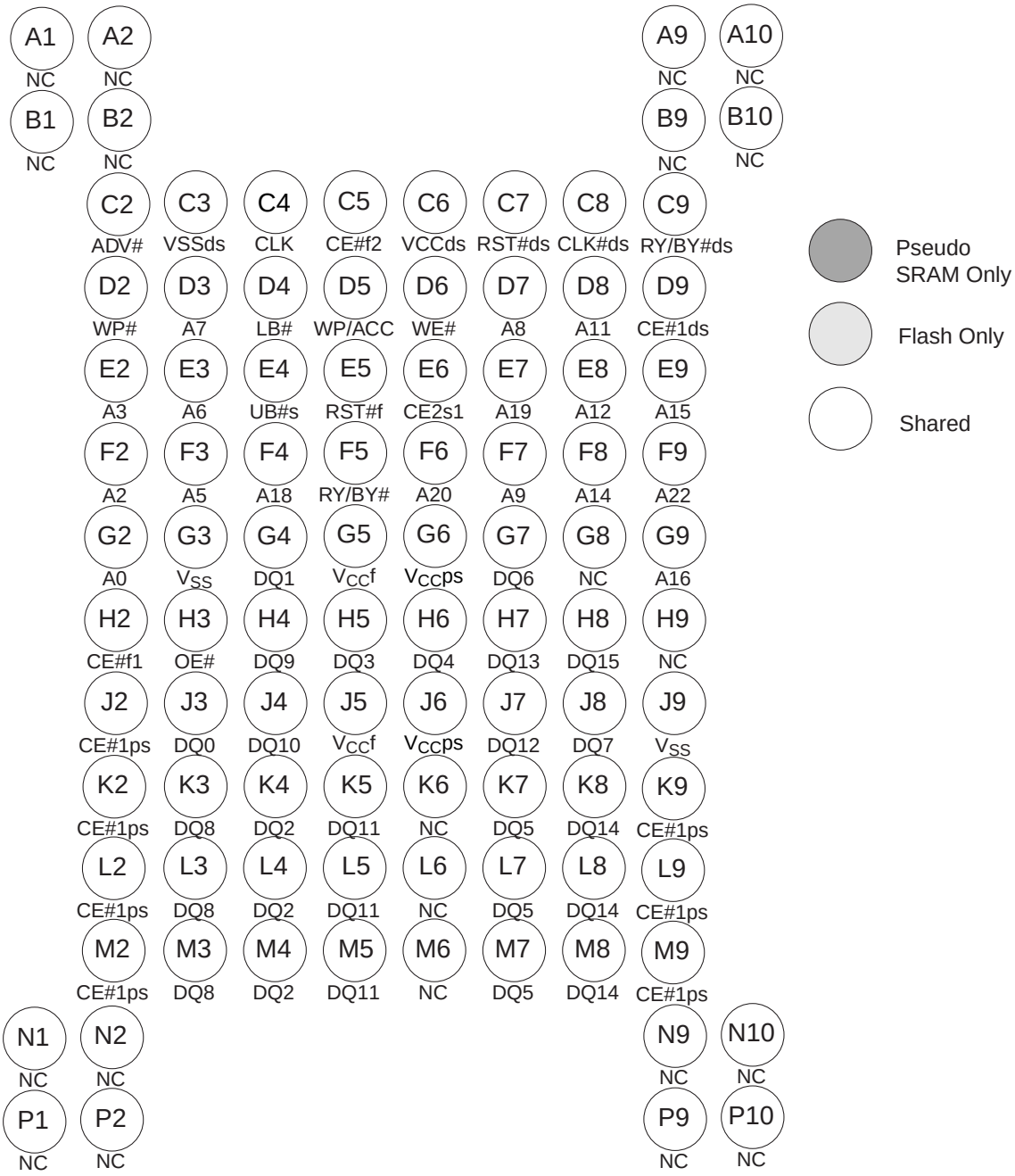
64-Ball Fine-Pitch (FBGA)
Top View, Balls Facing Down



Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP and BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

LOOK AHEAD PINOUT



In order to provide customers with a migration path to higher densities, as well as the option to stack more die in a package, FASL has prepared a standard pinout that supports:

- NOR Flash and SRAM densities up to 4 Gigabits
- NOR Flash and pSRAM densities up to 4 Gigabits
- NOR Flash and pSRAM and DATA STORAGE densities up to 4 Gigabits.

The signal locations of the resultant MCP device are shown above. Note that for different densities, the actual package outline may vary. However, any pinout in any MCP will be a subset of the pinout above.

In some cases, there may be outrigger balls in locations outside the grid shown above. In such cases, the user is recommended to treat these as RFU's, and not connect them to any other signal.

In case of any further inquiries about the above look-ahead pinout, please refer to the application note on this subject, or contact the appropriate AMD or Fujitsu sales office.

PIN DESCRIPTION

A22–A21 = 2 Address inputs (Flash)

A20–A0 = 21 Address inputs (Flash and pSRAM)

DQ14–DQ0 = 15 Data inputs/outputs

DQ15 = DQ15 (Data input/output)

CE#f = Chip Enable input (Flash)

CE1#ps, CE2ps=Chip Enable (pSRAM)

OE# = Output Enable input (Flash)

WE# = Write Enable input (Flash)

WP#/ACC = Hardware Write Protect input/Programming Acceleration input (Flash)

RESET#f = Hardware Reset Pin input (Flash)

$V_{CC}f$ = Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)

$V_{CC}ps$ = pSRAM Power Supply

V_{SS} = Device Ground

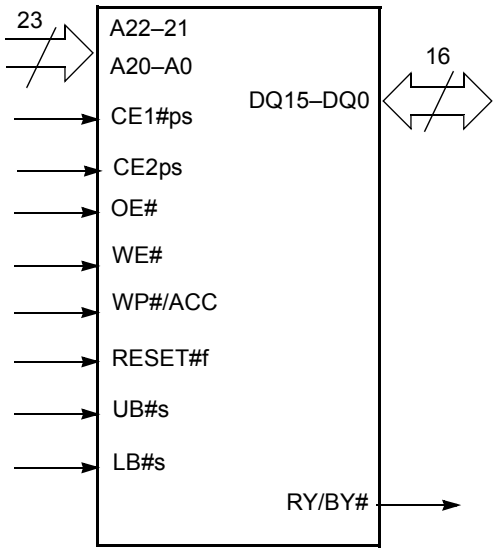
NC = Pin Not Connected Internally

UB#s = Upper Byte Control (pSRAM)

LB#s = Lower Byte Control (pSRAM)

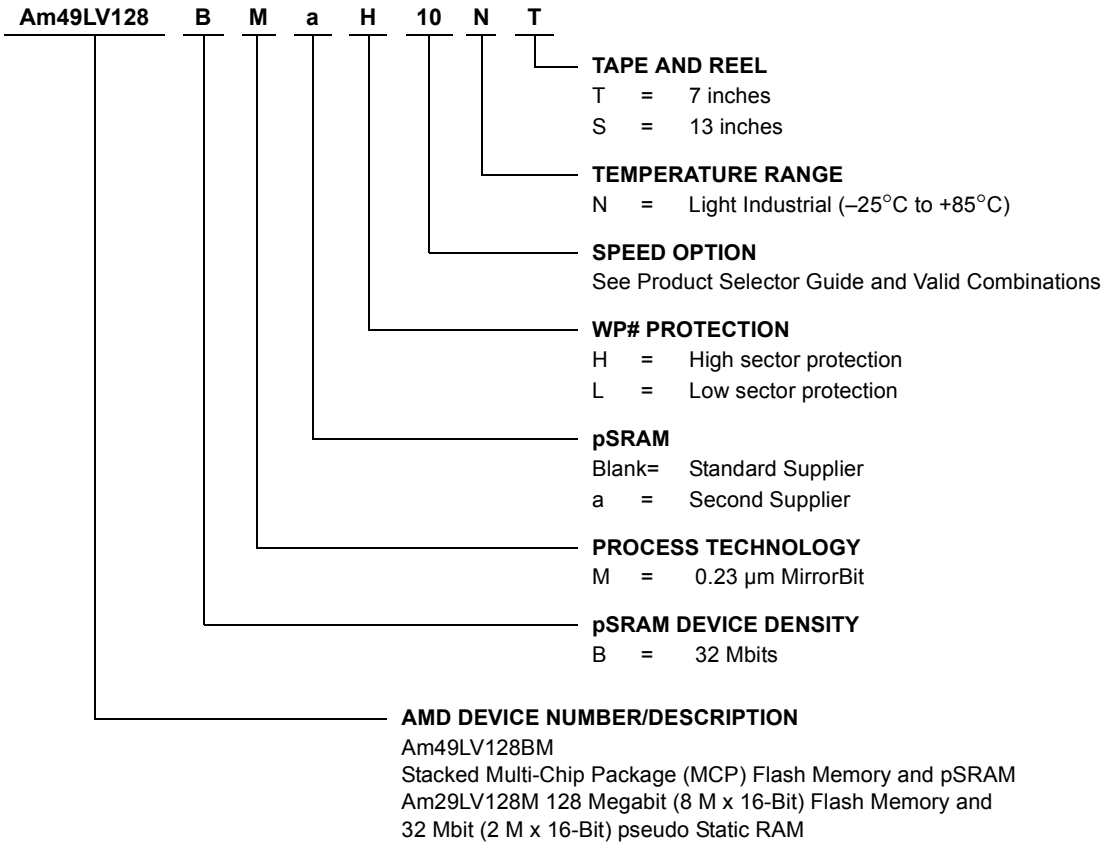
RY/BY# = Ready/Busy Output

LOGIC SYMBOL



ORDERING INFORMATION

The order number (Valid Combination) is formed by the following:



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#	ACC	Addresses (Note 2)	DQ0–DQ7	DQ8–DQ15
Read	L	L	H	H	X	X	A_{IN}	D_{OUT}	D_{OUT}
Write (Program/Erase)	L	H	L	H	(Note 3)	X	A_{IN}	(Note 4)	(Note 4)
Accelerated Program	L	H	L	H	(Note 3)	V_{HH}	A_{IN}	(Note 4)	(Note 4)
Standby	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V	X	H	X	High-Z	High-Z
Output Disable	L	H	H	H	X	X	X	High-Z	High-Z
Reset	X	X	X	L	X	X	X	High-Z	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	H	X	SA, A6 =L, A3=L, A2=L, A1=H, A0=L	(Note 4)	X
Sector Group Unprotect (Note 2)	L	H	L	V_{ID}	H	X	SA, A6=H, A3=L, A2=L, A1=H, A0=L	(Note 4)	X
Temporary Sector Group Unprotect	X	X	X	V_{ID}	H	X	A_{IN}	(Note 4)	(Note 4)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 11.5–12.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are A22:A0. Sector addresses are A22:A15 in both modes.*
2. *The sector group protect and sector group unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Unprotection" section.*
3. *If WP# = V_{IL}, the first or last sector remains protected. If WP# = V_{IH}, the first or last sector will be protected or unprotected as determined by the method described in "Write Protect (WP#)". All sectors are unprotected when shipped from the factory (The SecSi Sector may be factory protected depending on version ordered.)*
4. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 2).*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 14 for the timing diagram. Refer to the DC Characteristics table for the active current specification on reading array data.

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 4 words. The appropriate page is selected by the higher address bits A(max)–A2. Address bits A1–A0 determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the “read-page addresses” constant and changing the “intra-read page” addresses.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The “Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address space that each sector occupies.

Refer to the DC Characteristics table for the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Write Buffer

Write Buffer Programming allows the system write to a maximum of 16 words in one programming operation. This results in faster effective programming time than the standard programming algorithms. See “Write Buffer” for more information.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{IO} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{IO} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the DC Characteristics table for the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to the DC Characteristics table for the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 16 for the timing diagram.

V_{CC} Power-up and Power-down Sequencing

The device imposes no restrictions on V_{CC} power-up or power-down sequencing. Asserting RESET# to VIL is required during the entire V_{CC} power sequence until the respective supplies reach their operating voltages. Once V_{CC} attains its operating voltage, de-assertion of RESET# to V_{IH} is permitted.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Address Table

Sector	A22–A15								Sector Size (Kwords)	16-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	0	32	000000–007FFF
SA1	0	0	0	0	0	0	0	1	32	008000–00FFFF
SA2	0	0	0	0	0	0	1	0	32	010000–017FFF
SA3	0	0	0	0	0	0	1	1	32	018000–01FFFF
SA4	0	0	0	0	0	1	0	0	32	020000–027FFF
SA5	0	0	0	0	0	1	0	1	32	028000–02FFFF
SA6	0	0	0	0	0	1	1	0	32	030000–037FFF
SA7	0	0	0	0	0	1	1	1	32	038000–03FFFF
SA8	0	0	0	0	1	0	0	0	32	040000–047FFF
SA9	0	0	0	0	1	0	0	1	32	048000–04FFFF
SA10	0	0	0	0	1	0	1	0	32	050000–057FFF
SA11	0	0	0	0	1	0	1	1	32	058000–05FFFF
SA12	0	0	0	0	1	1	0	0	32	060000–067FFF
SA13	0	0	0	0	1	1	0	1	32	068000–06FFFF
SA14	0	0	0	0	1	1	1	0	32	070000–077FFF
SA15	0	0	0	0	1	1	1	1	32	078000–07FFFF
SA16	0	0	0	1	0	0	0	0	32	080000–087FFF
SA17	0	0	0	1	0	0	0	1	32	088000–08FFFF
SA18	0	0	0	1	0	0	1	0	32	090000–097FFF
SA19	0	0	0	1	0	0	1	1	32	098000–09FFFF
SA20	0	0	0	1	0	1	0	0	32	0A0000–0A7FFF
SA21	0	0	0	1	0	1	0	1	32	0A8000–0AFFFF
SA22	0	0	0	1	0	1	1	0	32	0B0000–0B7FFF
SA23	0	0	0	1	0	1	1	1	32	0B8000–0BFFFF
SA24	0	0	0	1	1	0	0	0	32	0C0000–0C7FFF
SA25	0	0	0	1	1	0	0	1	32	0C8000–0CFFFF
SA26	0	0	0	1	1	0	1	0	32	0D0000–0D7FFF
SA27	0	0	0	1	1	0	1	1	32	0D8000–0DFFFF
SA28	0	0	0	1	1	1	0	0	32	0E0000–0E7FFF

Table 2. Sector Address Table (Continued)

Sector	A22–A15								Sector Size (Kwords)	16-bit Address Range (in hexadecimal)
SA29	0	0	0	1	1	1	0	1	32	0E8000–0EFFFF
SA30	0	0	0	1	1	1	1	0	32	0F0000–0F7FFF
SA31	0	0	0	1	1	1	1	1	32	0F8000–0FFFFF
SA32	0	0	1	0	0	0	0	0	32	100000–107FFF
SA33	0	0	1	0	0	0	0	1	32	108000–10FFFF
SA34	0	0	1	0	0	0	1	0	32	110000–117FFF
SA35	0	0	1	0	0	0	1	1	32	118000–11FFFF
SA36	0	0	1	0	0	1	0	0	32	120000–127FFF
SA37	0	0	1	0	0	1	0	1	32	128000–12FFFF
SA38	0	0	1	0	0	1	1	0	32	130000–137FFF
SA39	0	0	1	0	0	1	1	1	32	138000–13FFFF
SA40	0	0	1	0	1	0	0	0	32	140000–147FFF
SA41	0	0	1	0	1	0	0	1	32	148000–14FFFF
SA42	0	0	1	0	1	0	1	0	32	150000–157FFF
SA43	0	0	1	0	1	0	1	1	32	158000–15FFFF
SA44	0	0	1	0	1	1	0	0	32	160000–167FFF
SA45	0	0	1	0	1	1	0	1	32	168000–16FFFF
SA46	0	0	1	0	1	1	1	0	32	170000–177FFF
SA47	0	0	1	0	1	1	1	1	32	178000–17FFFF
SA48	0	0	1	1	0	0	0	0	32	180000–187FFF
SA49	0	0	1	1	0	0	0	1	32	188000–18FFFF
SA50	0	0	1	1	0	0	1	0	32	190000–197FFF
SA51	0	0	1	1	0	0	1	1	32	198000–19FFFF
SA52	0	0	1	1	0	1	0	0	32	1A0000–1A7FFF
SA53	0	0	1	1	0	1	0	1	32	1A8000–1AFFFF
SA54	0	0	1	1	0	1	1	0	32	1B0000–1B7FFF
SA55	0	0	1	1	0	1	1	1	32	1B8000–1BFFFF
SA56	0	0	1	1	1	0	0	0	32	1C0000–1C7FFF
SA57	0	0	1	1	1	0	0	1	32	1C8000–1CFFFF
SA58	0	0	1	1	1	0	1	0	32	1D0000–1D7FFF
SA59	0	0	1	1	1	0	1	1	32	1D8000–1DFFFF
SA60	0	0	1	1	1	1	0	0	32	1E0000–1E7FFF
SA61	0	0	1	1	1	1	0	1	32	1E8000–1EFFFF
SA62	0	0	1	1	1	1	1	0	32	1F0000–1F7FFF
SA63	0	0	1	1	1	1	1	1	32	1F8000–1FFFFF
SA64	0	1	0	0	0	0	0	0	32	200000–207FFF
SA65	0	1	0	0	0	0	0	1	32	208000–20FFFF
SA66	0	1	0	0	0	0	1	0	32	210000–217FFF
SA67	0	1	0	0	0	0	1	1	32	218000–21FFFF
SA68	0	1	0	0	0	1	0	0	32	220000–227FFF
SA69	0	1	0	0	0	1	0	1	32	228000–22FFFF
SA70	0	1	0	0	0	1	1	0	32	230000–237FFF
SA71	0	1	0	0	0	1	1	1	32	238000–23FFFF
SA72	0	1	0	0	1	0	0	0	32	240000–247FFF
SA73	0	1	0	0	1	0	0	1	32	248000–24FFFF
SA74	0	1	0	0	1	0	1	0	32	250000–257FFF
SA75	0	1	0	0	1	0	1	1	32	258000–25FFFF
SA76	0	1	0	0	1	1	0	0	32	260000–267FFF

Table 2. Sector Address Table (Continued)

Sector	A22–A15								Sector Size (Kwords)	16-bit Address Range (in hexadecimal)
SA77	0	1	0	0	1	1	0	1	32	268000–26FFFF
SA78	0	1	0	0	1	1	1	0	32	270000–277FFF
SA79	0	1	0	0	1	1	1	1	32	278000–27FFFF
SA80	0	1	0	1	0	0	0	0	32	280000–287FFF
SA81	0	1	0	1	0	0	0	1	32	288000–28FFFF
SA82	0	1	0	1	0	0	1	0	32	290000–297FFF
SA83	0	1	0	1	0	0	1	1	32	298000–29FFFF
SA84	0	1	0	1	0	1	0	0	32	2A0000–2A7FFF
SA85	0	1	0	1	0	1	0	1	32	2A8000–2AFFFF
SA86	0	1	0	1	0	1	1	0	32	2B0000–2B7FFF
SA87	0	1	0	1	0	1	1	1	32	2B8000–2BFFFF
SA88	0	1	0	1	1	0	0	0	32	2C0000–2C7FFF
SA89	0	1	0	1	1	0	0	1	32	2C8000–2CFFFF
SA90	0	1	0	1	1	0	1	0	32	2D0000–2D7FFF
SA91	0	1	0	1	1	0	1	1	32	2D8000–2DFFFF
SA92	0	1	0	1	1	1	0	0	32	2E0000–2E7FFF
SA93	0	1	0	1	1	1	0	1	32	2E8000–2EFFFF
SA94	0	1	0	1	1	1	1	0	32	2F0000–2F7FFF
SA95	0	1	0	1	1	1	1	1	32	2F8000–2FFFFF
SA96	0	1	1	0	0	0	0	0	32	300000–307FFF
SA97	0	1	1	0	0	0	0	1	32	308000–30FFFF
SA98	0	1	1	0	0	0	1	0	32	310000–317FFF
SA99	0	1	1	0	0	0	1	1	32	318000–31FFFF
SA100	0	1	1	0	0	1	0	0	32	320000–327FFF
SA101	0	1	1	0	0	1	0	1	32	328000–32FFFF
SA102	0	1	1	0	0	1	1	0	32	330000–337FFF
SA103	0	1	1	0	0	1	1	1	32	338000–33FFFF
SA104	0	1	1	0	1	0	0	0	32	340000–347FFF
SA105	0	1	1	0	1	0	0	1	32	348000–34FFFF
SA106	0	1	1	0	1	0	1	0	32	350000–357FFF
SA107	0	1	1	0	1	0	1	1	32	358000–35FFFF
SA108	0	1	1	0	1	1	0	0	32	360000–367FFF
SA109	0	1	1	0	1	1	0	1	32	368000–36FFFF
SA110	0	1	1	0	1	1	1	0	32	370000–377FFF
SA111	0	1	1	0	1	1	1	1	32	378000–37FFFF
SA112	0	1	1	1	0	0	0	0	32	380000–387FFF
SA113	0	1	1	1	0	0	0	1	32	388000–38FFFF
SA114	0	1	1	1	0	0	1	0	32	390000–397FFF
SA115	0	1	1	1	0	0	1	1	32	398000–39FFFF
SA116	0	1	1	1	0	1	0	0	32	3A0000–3A7FFF
SA117	0	1	1	1	0	1	0	1	32	3A8000–3AFFFF
SA118	0	1	1	1	0	1	1	0	32	3B0000–3B7FFF
SA119	0	1	1	1	0	1	1	1	32	3B8000–3BFFFF
SA120	0	1	1	1	1	0	0	0	32	3C0000–3C7FFF
SA121	0	1	1	1	1	0	0	1	32	3C8000–3CFFFF
SA122	0	1	1	1	1	0	1	0	32	3D0000–3D7FFF
SA123	0	1	1	1	1	0	1	1	32	3D8000–3DFFFF
SA124	0	1	1	1	1	1	0	0	32	3E0000–3E7FFF

Table 2. Sector Address Table (Continued)

Sector	A22–A15								Sector Size (Kwords)	16-bit Address Range (in hexadecimal)
SA125	0	1	1	1	1	1	0	1	32	3E8000–3EFFFF
SA126	0	1	1	1	1	1	1	0	32	3F0000–3F7FFF
SA127	0	1	1	1	1	1	1	1	32	3F8000–3FFFFF
SA128	1	0	0	0	0	0	0	0	32	400000–407FFF
SA129	1	0	0	0	0	0	0	1	32	408000–40FFFF
SA130	1	0	0	0	0	0	1	0	32	410000–417FFF
SA131	1	0	0	0	0	0	1	1	32	418000–41FFFF
SA132	1	0	0	0	0	1	0	0	32	420000–427FFF
SA133	1	0	0	0	0	1	0	1	32	428000–42FFFF
SA134	1	0	0	0	0	1	1	0	32	430000–437FFF
SA135	1	0	0	0	0	1	1	1	32	438000–43FFFF
SA136	1	0	0	0	1	0	0	0	32	440000–447FFF
SA137	1	0	0	0	1	0	0	1	32	448000–44FFFF
SA138	1	0	0	0	1	0	1	0	32	450000–457FFF
SA139	1	0	0	0	1	0	1	1	32	458000–45FFFF
SA140	1	0	0	0	1	1	0	0	32	460000–467FFF
SA141	1	0	0	0	1	1	0	1	32	468000–46FFFF
SA142	1	0	0	0	1	1	1	0	32	470000–477FFF
SA143	1	0	0	0	1	1	1	1	32	478000–47FFFF
SA144	1	0	0	1	0	0	0	0	32	480000–487FFF
SA145	1	0	0	1	0	0	0	1	32	488000–48FFFF
SA146	1	0	0	1	0	0	1	0	32	490000–497FFF
SA147	1	0	0	1	0	0	1	1	32	498000–49FFFF
SA148	1	0	0	1	0	1	0	0	32	4A0000–4A7FFF
SA149	1	0	0	1	0	1	0	1	32	4A8000–4AFFFF
SA150	1	0	0	1	0	1	1	0	32	4B0000–4B7FFF
SA151	1	0	0	1	0	1	1	1	32	4B8000–4BFFFF
SA152	1	0	0	1	1	0	0	0	32	4C0000–4C7FFF
SA153	1	0	0	1	1	0	0	1	32	4C8000–4CFFFF
SA154	1	0	0	1	1	0	1	0	32	4D0000–4D7FFF
SA155	1	0	0	1	1	0	1	1	32	4D8000–4DFFFF
SA156	1	0	0	1	1	1	0	0	32	4E0000–4E7FFF
SA157	1	0	0	1	1	1	0	1	32	4E8000–4EFFFF
SA158	1	0	0	1	1	1	1	0	32	4F0000–4F7FFF
SA159	1	0	0	1	1	1	1	1	32	4F8000–4FFFFF
SA160	1	0	1	0	0	0	0	0	32	500000–507FFF
SA161	1	0	1	0	0	0	0	1	32	508000–50FFFF
SA162	1	0	1	0	0	0	1	0	32	510000–517FFF
SA163	1	0	1	0	0	0	1	1	32	518000–51FFFF
SA164	1	0	1	0	0	1	0	0	32	520000–527FFF
SA165	1	0	1	0	0	1	0	1	32	528000–52FFFF
SA166	1	0	1	0	0	1	1	0	32	530000–537FFF
SA167	1	0	1	0	0	1	1	1	32	538000–53FFFF
SA168	1	0	1	0	1	0	0	0	32	540000–547FFF
SA169	1	0	1	0	1	0	0	1	32	548000–54FFFF
SA170	1	0	1	0	1	0	1	0	32	550000–557FFF
SA171	1	0	1	0	1	0	1	1	32	558000–55FFFF
SA172	1	0	1	0	1	1	0	0	32	560000–567FFF

Table 2. Sector Address Table (Continued)

Sector	A22–A15								Sector Size (Kwords)	16-bit Address Range (in hexadecimal)
SA173	1	0	1	0	1	1	0	1	32	568000–56FFFF
SA174	1	0	1	0	1	1	1	0	32	570000–577FFF
SA175	1	0	1	0	1	1	1	1	32	578000–57FFFF
SA176	1	0	1	1	0	0	0	0	32	580000–587FFF
SA177	1	0	1	1	0	0	0	1	32	588000–58FFFF
SA178	1	0	1	1	0	0	1	0	32	590000–597FFF
SA179	1	0	1	1	0	0	1	1	32	598000–59FFFF
SA180	1	0	1	1	0	1	0	0	32	5A0000–5A7FFF
SA181	1	0	1	1	0	1	0	1	32	5A8000–5AFFFF
SA182	1	0	1	1	0	1	1	0	32	5B0000–5B7FFF
SA183	1	0	1	1	0	1	1	1	32	5B8000–5BFFFF
SA184	1	0	1	1	1	0	0	0	32	5C0000–5C7FFF
SA185	1	0	1	1	1	0	0	1	32	5C8000–5CFFFF
SA186	1	0	1	1	1	0	1	0	32	5D0000–5D7FFF
SA187	1	0	1	1	1	0	1	1	32	5D8000–5DFFFF
SA188	1	0	1	1	1	1	0	0	32	5E0000–5E7FFF
SA189	1	0	1	1	1	1	0	1	32	5E8000–5EFFFF
SA190	1	0	1	1	1	1	1	0	32	5F0000–5F7FFF
SA191	1	0	1	1	1	1	1	1	32	5F8000–5FFFFF
SA192	1	1	0	0	0	0	0	0	32	600000–607FFF
SA193	1	1	0	0	0	0	0	1	32	608000–60FFFF
SA194	1	1	0	0	0	0	1	0	32	610000–617FFF
SA195	1	1	0	0	0	0	1	1	32	618000–61FFFF
SA196	1	1	0	0	0	1	0	0	32	620000–627FFF
SA197	1	1	0	0	0	1	0	1	32	628000–62FFFF
SA198	1	1	0	0	0	1	1	0	32	630000–637FFF
SA199	1	1	0	0	0	1	1	1	32	638000–63FFFF
SA200	1	1	0	0	1	0	0	0	32	640000–647FFF
SA201	1	1	0	0	1	0	0	1	32	648000–64FFFF
SA202	1	1	0	0	1	0	1	0	32	650000–657FFF
SA203	1	1	0	0	1	0	1	1	32	658000–65FFFF
SA204	1	1	0	0	1	1	0	0	32	660000–667FFF
SA205	1	1	0	0	1	1	0	1	32	668000–66FFFF
SA206	1	1	0	0	1	1	1	0	32	670000–677FFF
SA207	1	1	0	0	1	1	1	1	32	678000–67FFFF
SA208	1	1	0	1	0	0	0	0	32	680000–687FFF
SA209	1	1	0	1	0	0	0	1	32	688000–68FFFF
SA210	1	1	0	1	0	0	1	0	32	690000–697FFF
SA211	1	1	0	1	0	0	1	1	32	698000–69FFFF
SA212	1	1	0	1	0	1	0	0	32	6A0000–6A7FFF
SA213	1	1	0	1	0	1	0	1	32	6A8000–6AFFFF
SA214	1	1	0	1	0	1	1	0	32	6B0000–6B7FFF
SA215	1	1	0	1	0	1	1	1	32	6B8000–6BFFFF
SA216	1	1	0	1	1	0	0	0	32	6C0000–6C7FFF
SA217	1	1	0	1	1	0	0	1	32	6C8000–6CFFFF
SA218	1	1	0	1	1	0	1	0	32	6D0000–6D7FFF
SA219	1	1	0	1	1	0	1	1	32	6D8000–6DFFFF
SA220	1	1	0	1	1	1	0	0	32	6E0000–6E7FFF

Table 2. Sector Address Table (Continued)

Sector	A22–A15								Sector Size (Kwords)	16-bit Address Range (in hexadecimal)
SA221	1	1	0	1	1	1	0	1	32	6E8000–6EFFFF
SA222	1	1	0	1	1	1	1	0	32	6F0000–6F7FFF
SA223	1	1	0	1	1	1	1	1	32	6F8000–6FFFFF
SA224	1	1	1	0	0	0	0	0	32	700000–707FFF
SA225	1	1	1	0	0	0	0	1	32	708000–70FFFF
SA226	1	1	1	0	0	0	1	0	32	710000–717FFF
SA227	1	1	1	0	0	0	1	1	32	718000–71FFFF
SA228	1	1	1	0	0	1	0	0	32	720000–727FFF
SA229	1	1	1	0	0	1	0	1	32	728000–72FFFF
SA230	1	1	1	0	0	1	1	0	32	730000–737FFF
SA231	1	1	1	0	0	1	1	1	32	738000–73FFFF
SA232	1	1	1	0	1	0	0	0	32	740000–747FFF
SA233	1	1	1	0	1	0	0	1	32	748000–74FFFF
SA234	1	1	1	0	1	0	1	0	32	750000–757FFF
SA235	1	1	1	0	1	0	1	1	32	758000–75FFFF
SA236	1	1	1	0	1	1	0	0	32	760000–767FFF
SA237	1	1	1	0	1	1	0	1	32	768000–76FFFF
SA238	1	1	1	0	1	1	1	0	32	770000–777FFF
SA239	1	1	1	0	1	1	1	1	32	778000–77FFFF
SA240	1	1	1	1	0	0	0	0	32	780000–787FFF
SA241	1	1	1	1	0	0	0	1	32	788000–78FFFF
SA242	1	1	1	1	0	0	1	0	32	790000–797FFF
SA243	1	1	1	1	0	0	1	1	32	798000–79FFFF
SA244	1	1	1	1	0	1	0	0	32	7A0000–7A7FFF
SA245	1	1	1	1	0	1	0	1	32	7A8000–7AFFFF
SA246	1	1	1	1	0	1	1	0	32	7B0000–7B7FFF
SA247	1	1	1	1	0	1	1	1	32	7B8000–7BFFFF
SA248	1	1	1	1	1	0	0	0	32	7C0000–7C7FFF
SA249	1	1	1	1	1	0	0	1	32	7C8000–7CFFFF
SA250	1	1	1	1	1	0	1	0	32	7D0000–7D7FFF
SA251	1	1	1	1	1	0	1	1	32	7D8000–7DFFFF
SA252	1	1	1	1	1	1	0	0	32	7E0000–7E7FFF
SA253	1	1	1	1	1	1	0	1	32	7E8000–7EFFFF
SA254	1	1	1	1	1	1	1	0	32	7F0000–7F7FFF
SA255	1	1	1	1	1	1	1	1	32	7F8000–7FFFFF

SecSi (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 256 bytes in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

AMD offers the device with the SecSi Sector either customer lockable (standard shipping option) or factory locked (contact an AMD sales representative for ordering information). The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the SecSi Sector Indicator Bit permanently set to a “0.” The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a “1.” Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked. *Note that the ACC*

function and unlock bypass modes are not available when the SecSi Sector is enabled.

The SecSi sector address space in this device is allocated as follows:

Table 3. SecSi Sector Contents

SecSi Sector Address Range	Customer Lockable	ESN Factory Locked	ExpressFlash Factory Locked
000000h–000007h	Determined by customer	ESN	ESN or determined by customer
000008h–00007Fh		Unavailable	Determined by customer

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte SecSi sector.

The system may program the SecSi Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions.

Programming and protecting the SecSi Sector must be used with caution since, once protected, there is no procedure available for unprotecting the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 3.

Once the SecSi Sector is programmed, locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing within the remainder of the array.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In devices with an ESN, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. An ESN Factory Locked device has an 16-byte random ESN at addresses 000000h–000007h. Please contact your local AMD sales representative for details on ordering ESN Factory Locked devices.

Customers may opt to have their code programmed by AMD through the AMD ExpressFlash service (Express Flash Factory Locked). The devices are then shipped from AMD's factory with the SecSi Sector permanently locked. Contact an AMD representative for details on using AMD's ExpressFlash service.

Note: MCP devices with second supplier pSRAM have 000000h address programmed to 0000h data.

Sector Group Protection and Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection can be implemented via two methods.

Sector group protection/unprotection requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 24 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector group unprotect, all unprotected sector group must first be protected prior to the first sector group unprotect write cycle.

The device is shipped with all sector groups unprotected. AMD offers the option of programming and protecting sector groups at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector group is protected or unprotected. See the Sector Group Protection and Unprotection section for details.

Table 4. Sector Group Protection/Unprotection Address Table

Sector Group	A22–A15
SA0	00000000
SA1	00000001
SA2	00000010
SA3	00000011
SA4–SA7	000001xx
SA8–SA11	000010xx
SA12–SA15	000011xx
SA16–SA19	000100xx
SA20–SA23	000101xx
SA24–SA27	000110xx
SA28–SA31	000111xx
SA32–SA35	001000xx
SA36–SA39	001001xx
SA40–SA43	001010xx
SA44–SA47	001011xx
SA48–SA51	001100xx
SA52–SA55	001101xx
SA56–SA59	001110xx
SA60–SA63	001111xx
SA64–SA67	010000xx
SA68–SA71	010001xx
SA72–SA75	010010xx
SA76–SA79	010011xx
SA80–SA83	010100xx
SA84–SA87	010101xx
SA88–SA91	010110xx
SA92–SA95	010111xx
SA96–SA99	011000xx
SA100–SA103	011001xx
SA104–SA107	011010xx
SA108–SA111	011011xx
SA112–SA115	011100xx
SA116–SA119	011101xx
SA120–SA123	011110xx
SA124–SA127	011111xx
SA128–SA131	100000xx
SA132–SA135	100001xx
SA136–SA139	100010xx
SA140–SA143	100011xx
SA144–SA147	100100xx
SA148–SA151	100101xx
SA152–SA155	100110xx
SA156–SA159	100111xx
SA160–SA163	101000xx
SA164–SA167	101001xx
SA168–SA171	101010xx
SA172–SA175	101011xx
SA176–SA179	101100xx
SA180–SA183	101101xx
SA184–SA187	101110xx
SA188–SA191	101111xx
SA192–SA195	110000xx
SA196–SA199	110001xx
SA200–SA203	110010xx
SA204–SA207	110011xx
SA208–SA211	110100xx
SA212–SA215	110101xx
SA216–SA219	110110xx
SA220–SA223	110111xx
SA224–SA227	111000xx
SA228–SA231	111001xx
SA232–SA235	111010xx
SA236–SA239	111011xx
SA240–SA243	111100xx
SA244–SA247	111101xx
SA248–SA251	111110xx
SA252	11111100
SA253	11111101
SA254	11111110
SA255	11111111

Write Protect (WP#)

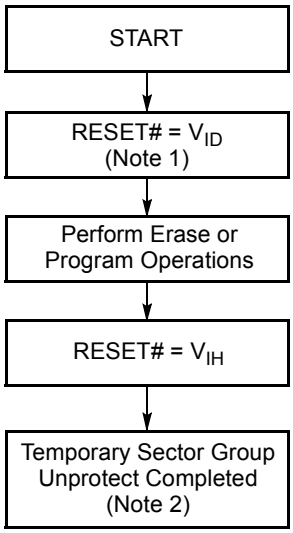
The Write Protect function provides a hardware method of protecting the last sector without using V_{ID}. Write Protect is one of two functions provided by the WP#/ACC input.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the last sector independently of whether those sectors were protected or unprotected using the method described in “Sector Group Protection and Unprotection”. Note that if WP#/ACC is at V_{IL} when the device is in the standby mode, the maximum input load current is increased. See the table in “DC Characteristics”.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the last sector was previously set to be protected or unprotected using the method described in “Sector Group Protection and Unprotection”. *Note that WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to VID. During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sector groups are protected again. Figure 1 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature.



Notes:

1. *All protected sector groups unprotected (If WP# = V_{IL}, the last sector group will remain protected).*
2. *All previously protected sector groups are protected once again.*

Figure 1. Temporary Sector Group Unprotect Operation

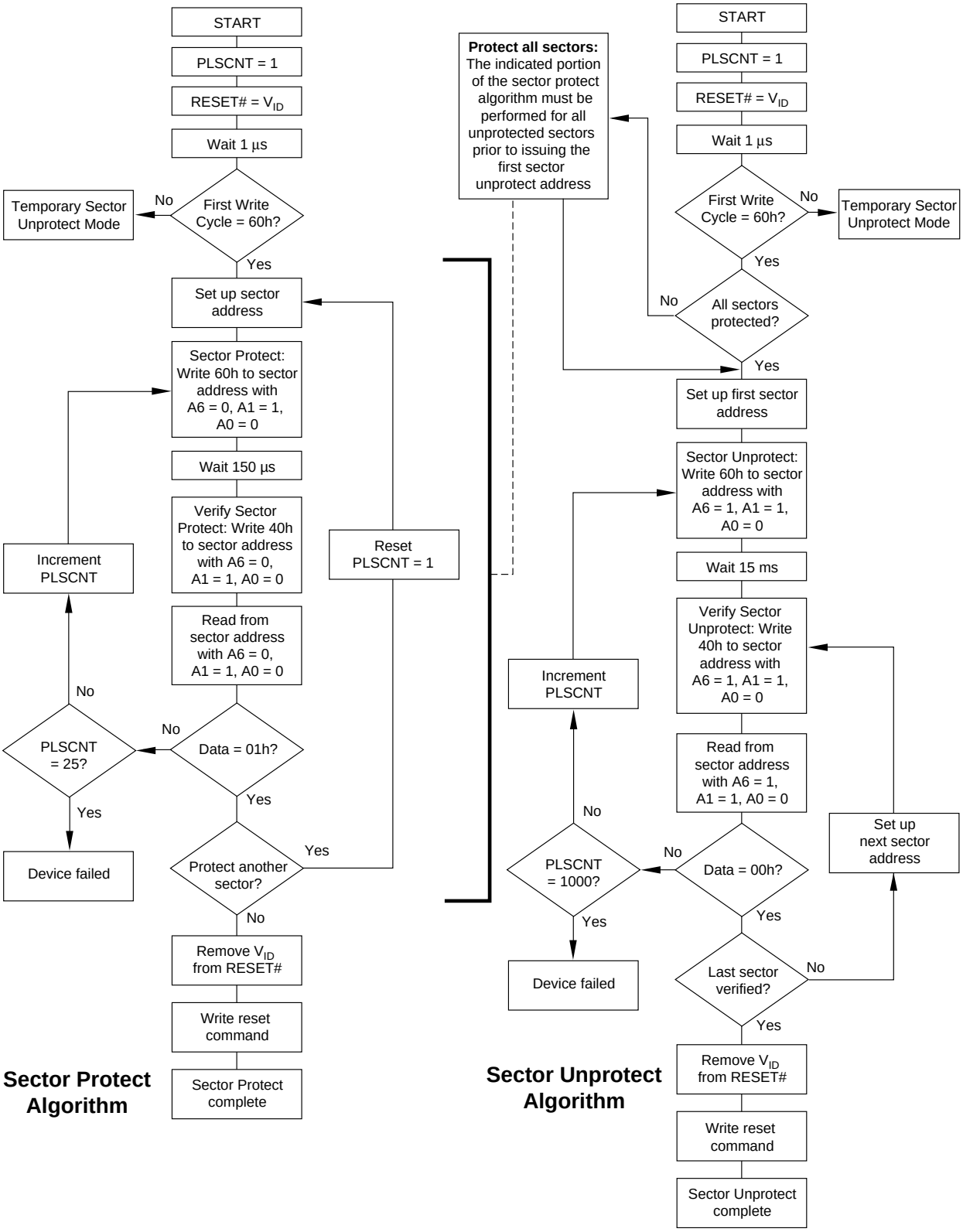


Figure 2. In-System Sector Group Protect/Unprotect Algorithms

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 9 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 5–8. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 5–8. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact an AMD representative for copies of these documents.

Table 5. CFI Query Identification String

Addresses (x16)	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 6. System Interface String

Addresses (x16)	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0007h	Typical timeout per single byte/word write 2^N µs
20h	0007h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	000Ah	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0001h	Max. timeout for byte/word write 2^N times typical
24h	0005h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 7. Device Geometry Definition

Addresses (x16)	Data	Description
27h	0018h	Device Size = 2^N byte
28h 29h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0005h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0001h	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	00FFh 0000h 0000h 0001h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information (refer to CFI publication 100)
35h 36h 37h 38h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

Table 8. Primary Vendor-Specific Extended Query

Addresses (x16)	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0008h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0010b = 0.23 µm MirrorBit
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0004h	Sector Protect/Unprotect scheme 04 = 29LV800 mode
4Ah	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors in Bank
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0001h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0004h/ 0005h	Top/Bottom Boot Sector Flag 00h = Uniform Device without WP# protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 9 defines the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state.* A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-

suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations table provides the read parameters, and Figure 14 shows the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Tables 9 show the address and data requirements. The autoselect command sequence may be written to an address that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence:

- A read cycle at address XX00h returns the manufacturer code.
- Three read cycles at addresses 01h, 0Eh, and 0Fh return the device code.
- A read cycle to an address containing a sector address (SA), and the address 02h on A7–A0 in word mode returns 01h if the sector is protected, or 00h if it is unprotected.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Enter SecSi Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing an 8-word random Electronic Serial Number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. Tables 9 show the address and data requirements for both command sequences. See also "SecSi (Secured Silicon) Sector Flash Memory Region" for further information. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Tables 9 show the address and data requirements for the word program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.* The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Tables 9 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle must contain the data 00h. The device then returns to the read mode.

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}–A_4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

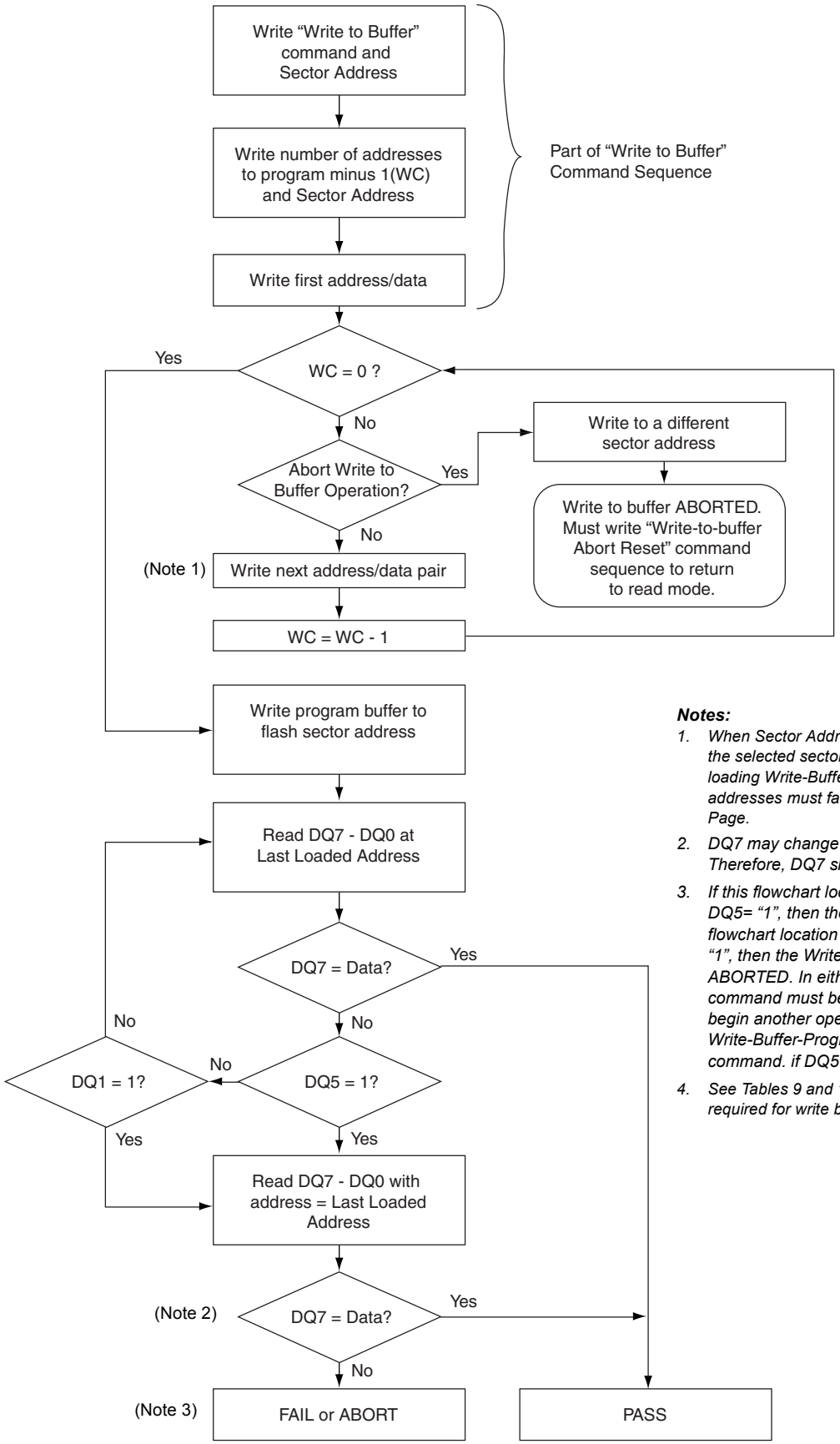
The abort condition is indicated by DQ1 = 1, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Accelerated Program

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the* WP#/*ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

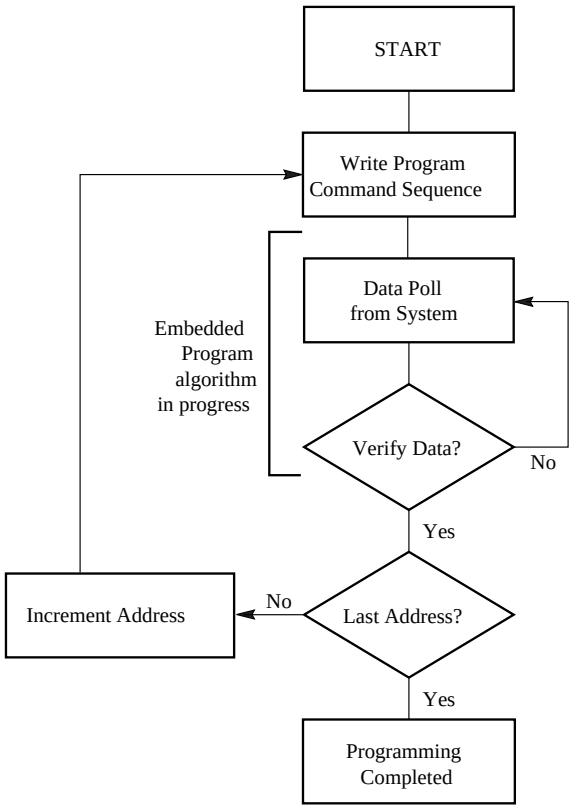
Figure 5 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 17 for timing diagrams.



Notes:

1. *When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.*
2. *DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.*
3. *If this flowchart location was reached because DQ5= "1", then the device FAILED. If this flowchart location was reached because DQ1= "1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If DQ1=1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5=1, write the Reset command.*
4. *See Tables 9 and 10 for command sequences required for write buffer programming.*

Figure 3. Write Buffer Programming Operation



Note: *See Tables 9 and 10 for program command sequence.*

Figure 4. Program Operation

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. Within the suspended sector, data may be read from addresses outside of the page (for example, Amax–A4) being programmed. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 µs maximum (5 µs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector or from selected addresses within the suspended sector (see previous paragraph). The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any sectors not in Erase Suspend or Program Suspend. If a read is needed from the SecSi Sector area (One-time Program area), then the user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

There is no time-out limit for the Program Suspend command. After the Program Suspend command is written, the device will stay in Program Suspend mode until the Program Resume command or the RESET command/operation is written.

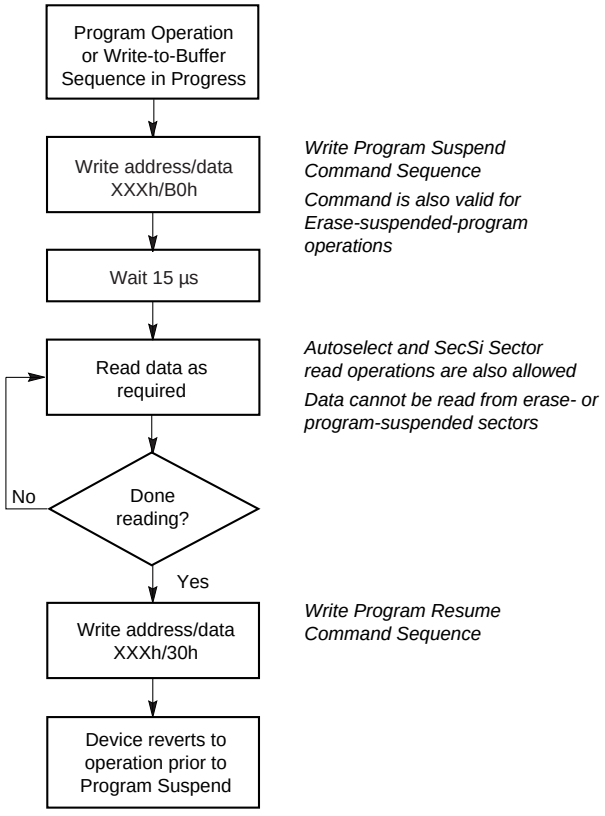


Figure 5. Program Suspend/Program Resume

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 9 show the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.* However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 19 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 10 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.* The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 19 section for timing diagrams.

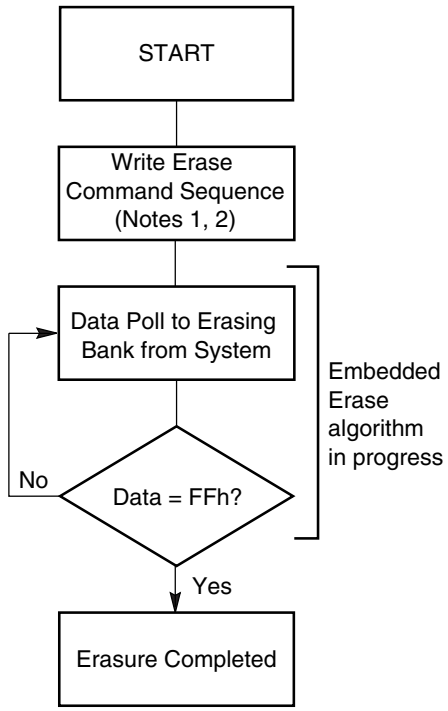


Figure 6. Erase Operation

Notes:

1. *See Tables 9 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5 µs (maximum of 20 µs) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

There is no time-out limit for the Erase Suspend command. After the Erase Suspend command is written, the device will stay in Erase Suspend mode until the Erase Resume command or the RESET command/operation is written.

Command Definitions

Table 9. Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
	Device ID (Note 9)	4	555	AA	2AA	55	555	90	X01	227E	X0E	2212	X0F	2200
	SecSi™ Sector Factory Protect (Note 10)	4	555	AA	2AA	55	555	90	X03	(Note 10)				
	Sector Group Protect Verify (Note 12)	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
Enter SecSi Sector Region		3	555	AA	2AA	55	555	88						
Exit SecSi Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (Note 11)		3	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (Note 13)		3	555	AA	2AA	55	555	F0						
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 14)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 15)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (Note 16)		1	BA	B0										
Program/Erase Resume (Note 17)		1	BA	30										
CFI Query (Note 18)		1	55	98										

Legend:

X = Don't care

RA = Read Address of the memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A22–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, and WC.*
5. *Unless otherwise noted, address bits A22–A11 are don't cares.*
6. *No unlock or command cycles required when device is in read mode.*
7. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high while the device is providing status information.*
8. *The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See the Autoselect Command Sequence section for more information.*
9. *The device ID must be read in three cycles.*
10. *If WP# protects the highest address sector, the data is 98H for factory locked and 18H for not factory locked. If WP# protects the lowest address sector, the data is 88H for factory locked and 08H for not factory locked.*
11. *The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 21.*
12. *The data is 00h for an unprotected sector and 01h for a protected sector.*
13. *Command sequence resets device for next command after aborted write-to-buffer operation.*
14. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
15. *The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.*
16. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
17. *The Erase Resume command is valid only during the Erase Suspend mode.*
18. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 10 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

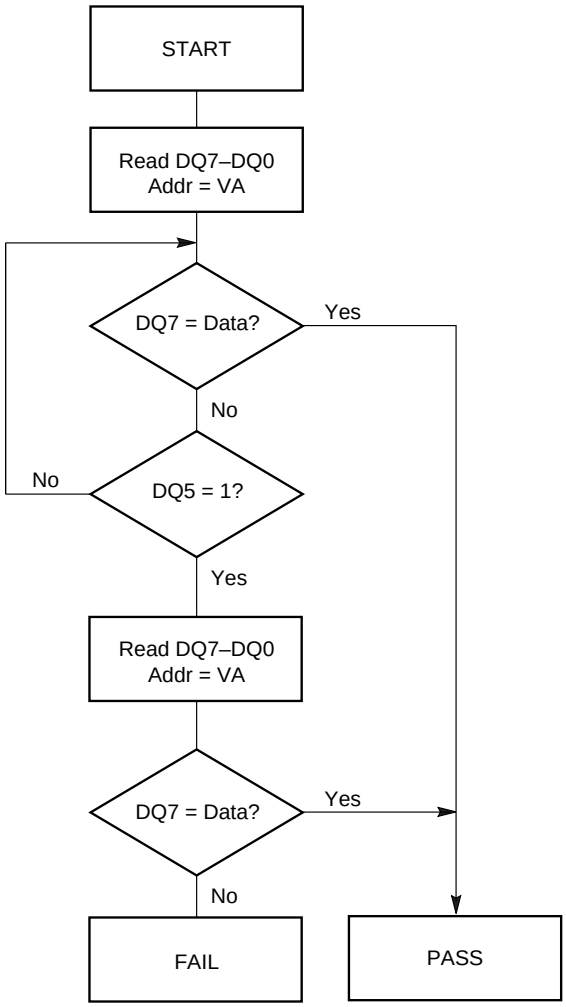
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 10 shows the outputs for Data# Polling on DQ7. Figure 8 shows the Data# Polling algorithm. Figure 20 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 7. Data# Polling Algorithm

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase

Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

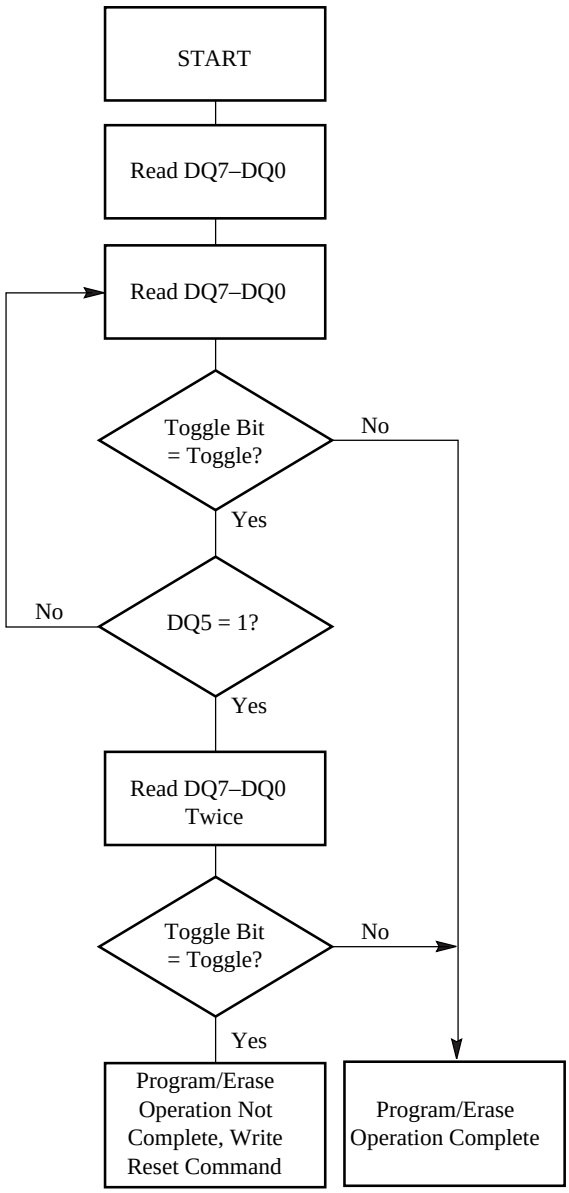
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 10 shows the outputs for Toggle Bit I on DQ6. Figure 9 shows the toggle bit algorithm. Figure 21 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 22 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note: *The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the subsections on DQ6 and DQ2 for more information.*

Figure 8. Toggle Bit Algorithm

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 10 to compare outputs for DQ2 and DQ6.

Figure 9 shows the toggle bit algorithm in flowchart form, and the section “DQ2: Toggle Bit II” explains the algorithm. Figure 21 shows the toggle bit timing diagram. Figure 22 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 9 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 9).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.”

In all these cases, the system must write the reset command (or the Unlock Bypass Reset command if in Unlock Bypass mode) to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 10 shows the status of DQ3 relative to the other status bits.

DQ1: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a “1”. The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer Programming section for more details.

Table 10. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)					
		Non-Program Suspended Sector	Data					
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A
		Non-Erase Suspended Sector	Data					
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A
Write-to-Buffer	Busy (Note 3)		DQ7#	Toggle	0	N/A	N/A	0
	Abort (Note 4)		DQ7#	Toggle	0	N/A	N/A	1

Notes:

1. *DQ5 switches to '1' when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.*
4. *DQ1 switches to '1' when the device has aborted the write-to-buffer operation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

V_{IO} . . . . . –0.5 V to +4.0 V

A9, OE#, ACC, and RESET#
(Note 2) . . . . . –0.5 V to +12.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 10. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 11.*
2. *Minimum DC input voltage on pins A9, OE#, ACC, and RESET# is –0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 10. Maximum DC input voltage on pin A9, OE#, ACC, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

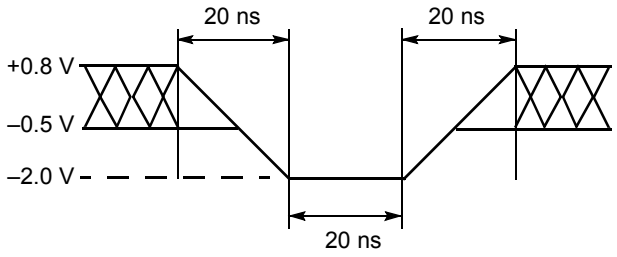


Figure 9. Maximum Negative Overshoot Waveform

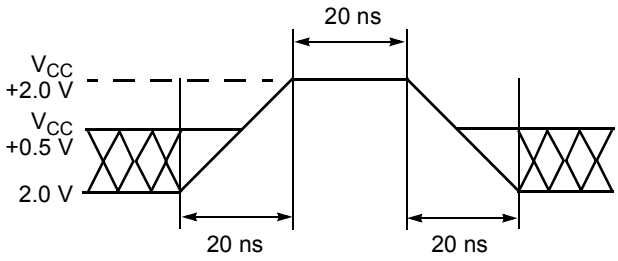


Figure 10. Maximum Positive Overshoot Waveform

OPERATING RANGES

Light Industrial (N) Devices

Ambient Temperature (T_A) . . . . . –25°C to +85°C

Supply Voltages

V_{CC} . . . . . 2.7–3.1 V

Note: *Operating ranges define those limits between which the functionality of the device is guaranteed.*

FLASH DC CHARACTERISTICS

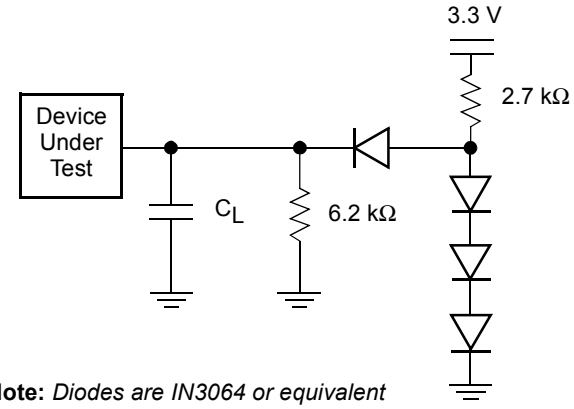
CMOS Compatible

Parameter Symbol	Parameter Description (Notes)	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	ACC Input Load Current	$V_{CC} = V_{CC\ max}$				35	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\ max}$; RESET# = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		15	20	mA
			1 MHz		15	20	
I_{CC2}	V_{CC} Initial Page Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}			30	50	mA
I_{CC3}	V_{CC} Intra-Page Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}			10	20	mA
I_{CC4}	V_{CC} Active Write Current (3, 4)	CE# = V_{IL}, OE# = V_{IH}			50	60	mA
I_{CC5}	V_{CC} Standby Current (3)	CE#, RESET# = V_{CC} ± 0.3 V, WP# = V_{IH}			1	5	µA
I_{CC6}	V_{CC} Reset Current (3)	RESET# = V_{SS} ± 0.3 V, WP# = V_{IH}			1	5	µA
I_{CC7}	Automatic Sleep Mode (3, 5)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V, WP# = V_{IH}			1	5	µA
V_{IL}	Input Low Voltage 1(6, 7)			–0.5		0.8	V
V_{IH}	Input High Voltage 1 (6, 7)			1.9		V_{CC} + 0.5	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 2.7–3.1 V		11.5		12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 2.7–3.1 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min} = V_{IO}$				0.15 x V_{IO}	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min} = V_{IO}$		0.85 V_{IO}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min} = V_{IO}$		V_{IO}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (7)			2.3		2.5	V

Notes:

1. *On the WP#/ACC pin only, the maximum input load current when WP# = V_{IL} is ± 5.0 µA.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.*
6. *If $V_{IO} < V_{CC}$, maximum V_{IL} for CE# and DQ I/Os is 0.3 V_{IO}. Maximum V_{IH} for these connections is V_{IO} + 0.3 V*
7. *V_{CC} voltage requirements.*
8. *V_{IO} voltage requirements.*
9. *Not 100% tested.*

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

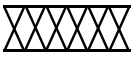
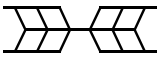
Figure 11. Test Setup

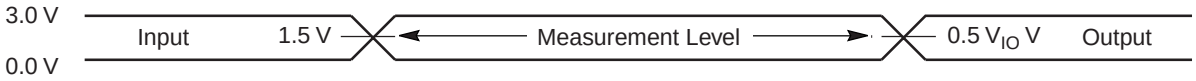
Table 11. Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels (See Note)	1.5	V
Output timing measurement reference levels	0.5 V_{IO}	V

Note: *If $V_{IO} < V_{CC}$, the reference level is 0.5 V_{IO}.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)



Note: *If $V_{IO} < V_{CC}$, the input measurement reference level is 0.5 V_{IO}.*

Figure 12. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	50	µs
t_{RSTH}	RESET# Low Hold Time	Min	50	µs

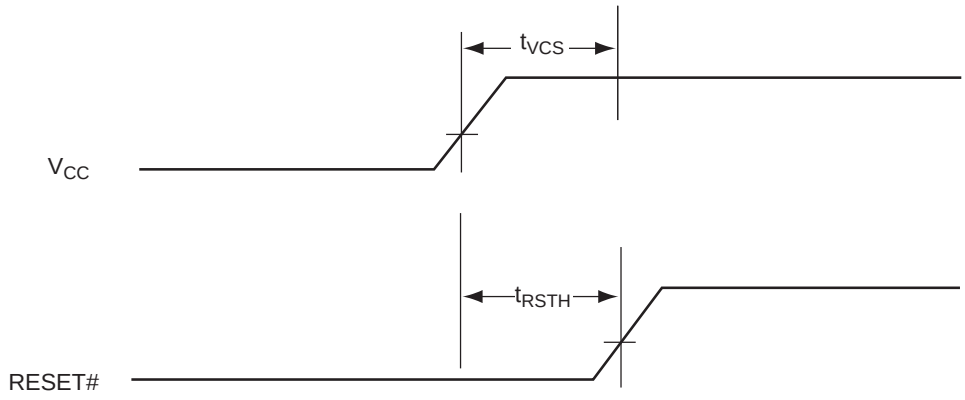


Figure 13. V_{CC} Power-up Diagram

AC CHARACTERISTICS

Flash Read-Only Operations

Parameter		Description		Test Setup		15	11	Unit
JEDEC	Std.							
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	105	110	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	105	110	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	105	110	ns
	t_{PACC}	Page Access Time			Max	25	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	30	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output Bus Release (Note 1)			Max	14		ns
t_{GHQZ}	t_{DF}	Output Enable to Output Bus Release (Note 1)			Max	14		ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0		ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns

Notes:

1. *Not 100% tested.*
2. *See Figure 12 and Table 11 for test specifications.*
3. *AC Specifications are tested with $V_{IO} = V_{CC}$. Contact AMD for information on AC operations with $V_{IO} \neq V_{CC}$.*

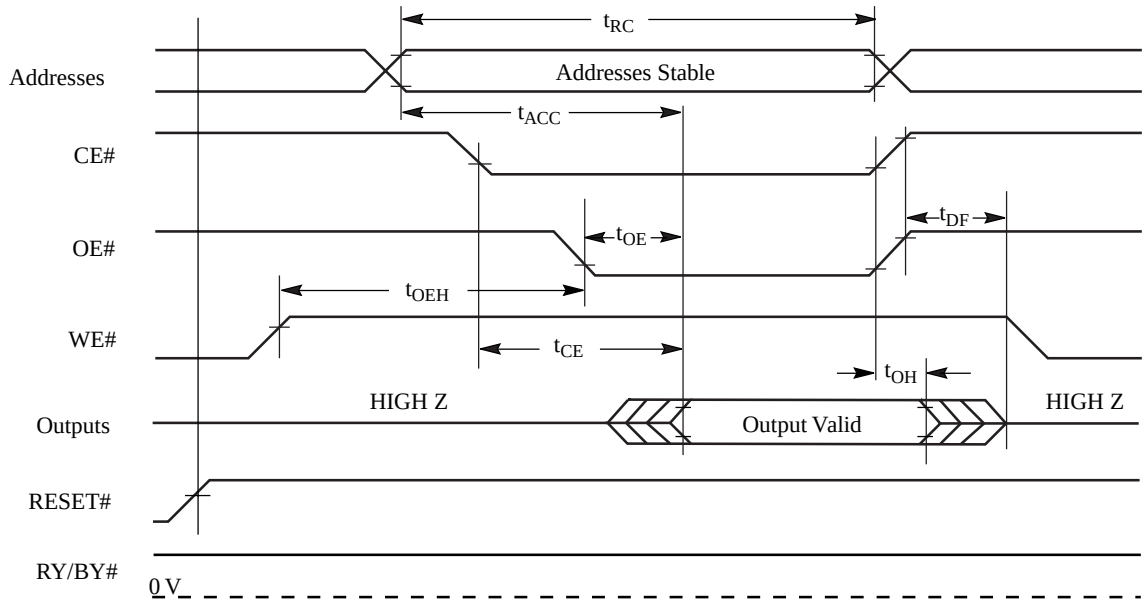


Figure 14. Read Operations Timings

AC CHARACTERISTICS

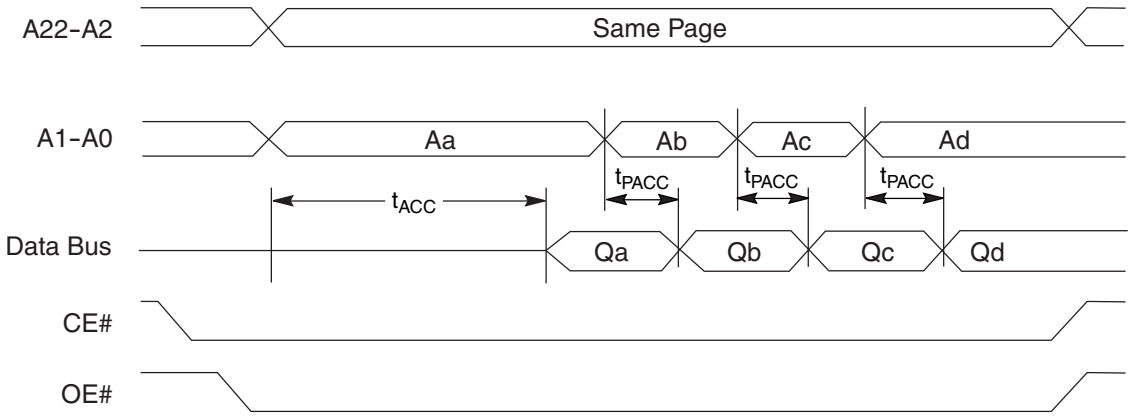


Figure 15. Page Read Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description			Unit
JEDEC	Std.				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note: *Not 100% tested.*

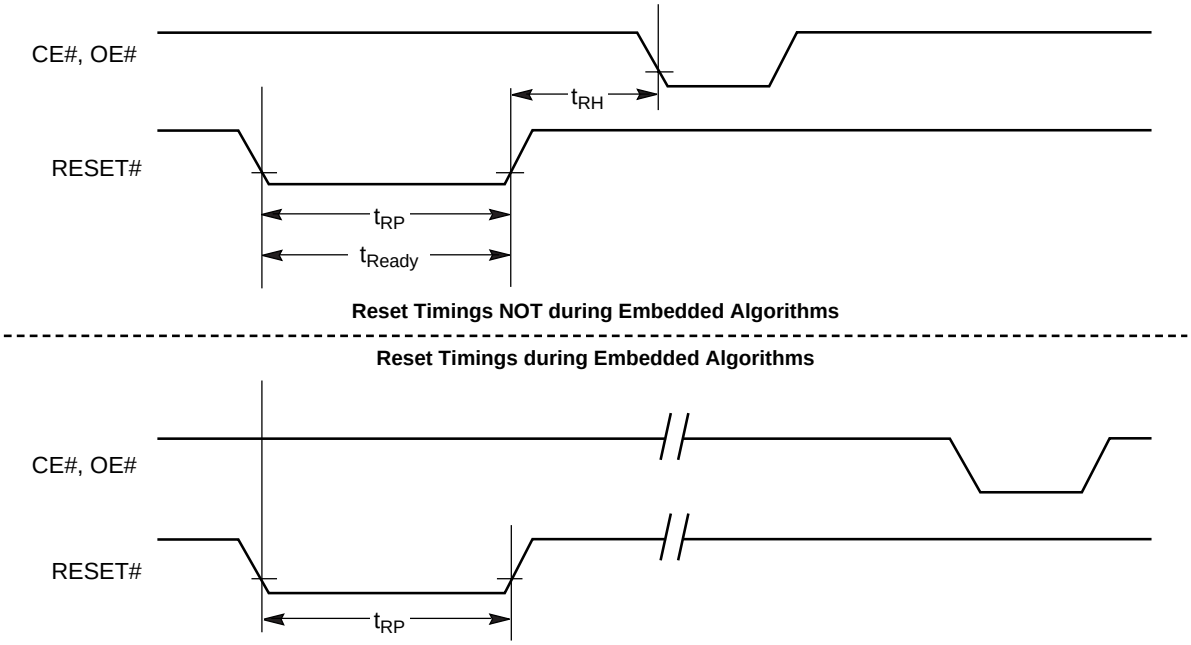


Figure 16. Reset Timings

AC CHARACTERISTICS

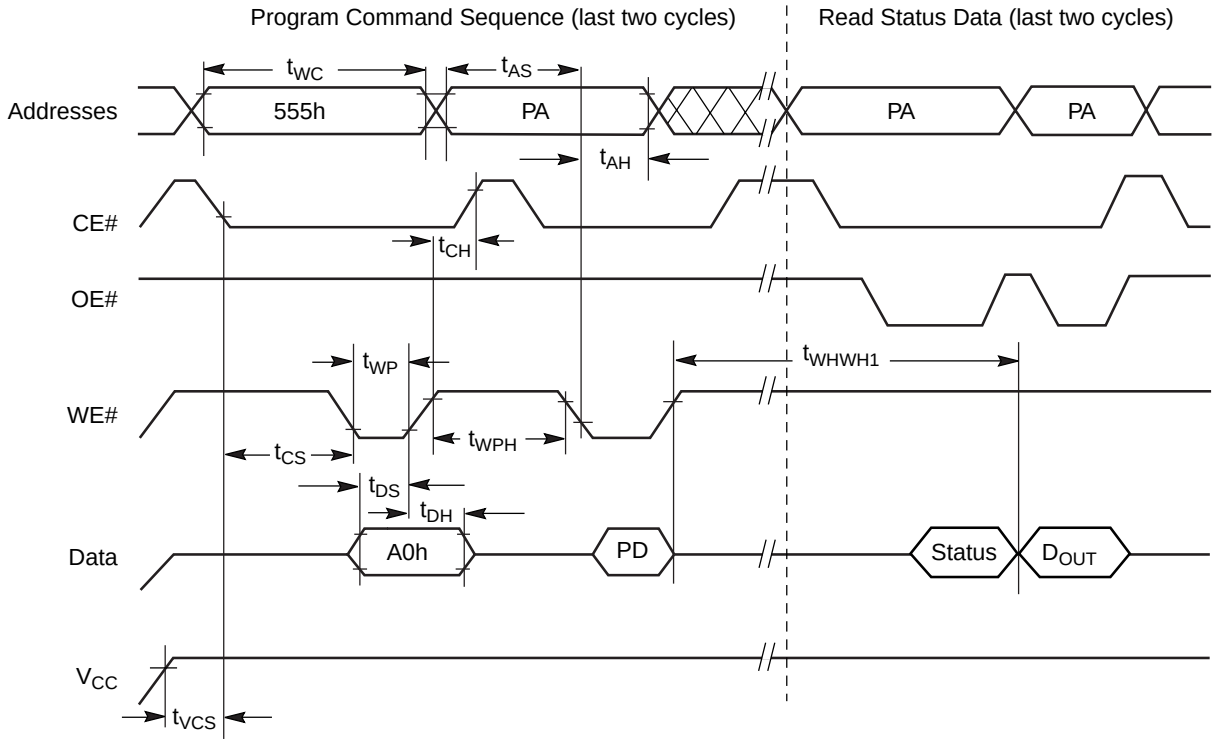
Erase and Program Operations

Parameter		Description			15	11	Unit
JEDEC	Std.						
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	105	110	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45		ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0		ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45		ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35		ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30		ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240		µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15		µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	11.8		µs
		Program Operation (Note 2)	Word	Typ	60		µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5		sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)		Min	250		ns
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50		µs

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*
3. *For 1–16 words.*
4. *Effective write buffer specification is based upon a 16-word write buffer operation.*

AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 17. Program Operation Timings

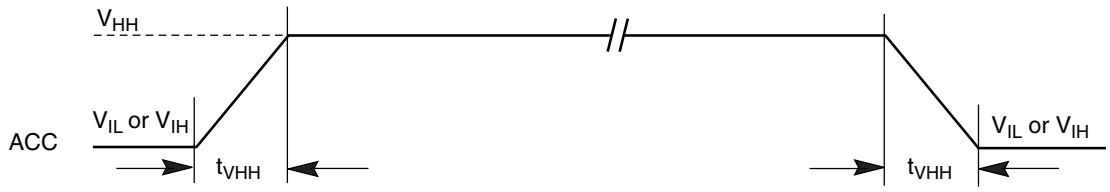
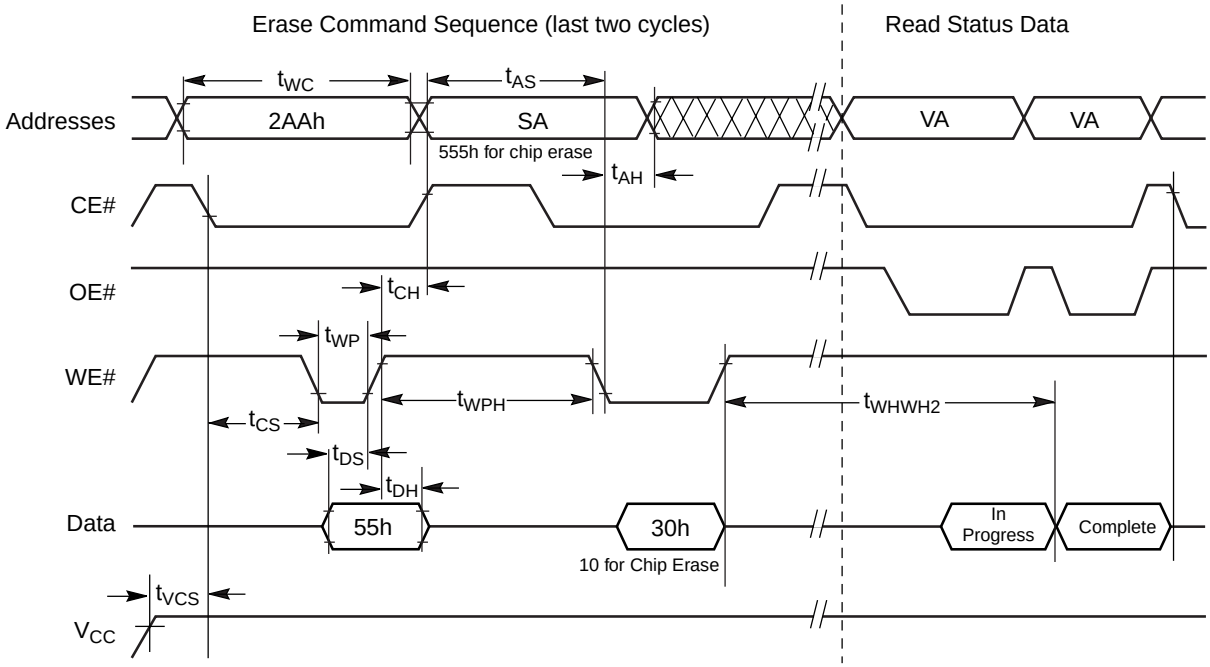


Figure 18. Accelerated Program Timing Diagram

AC CHARACTERISTICS

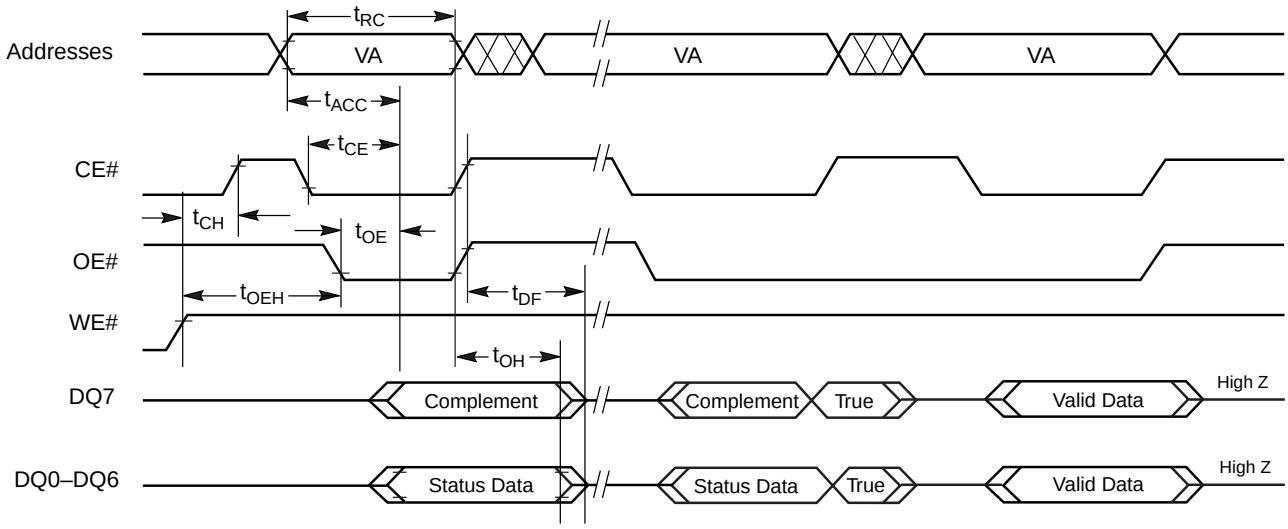


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status".*
2. *These waveforms are for the word mode.*

Figure 19. Chip/Sector Erase Operation Timings

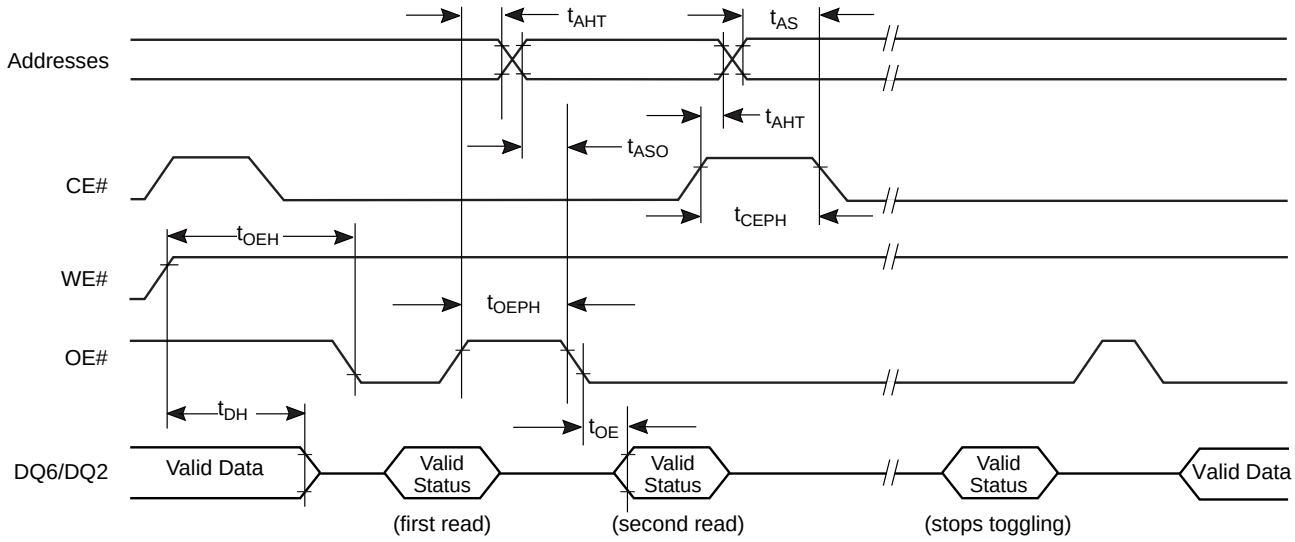
AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

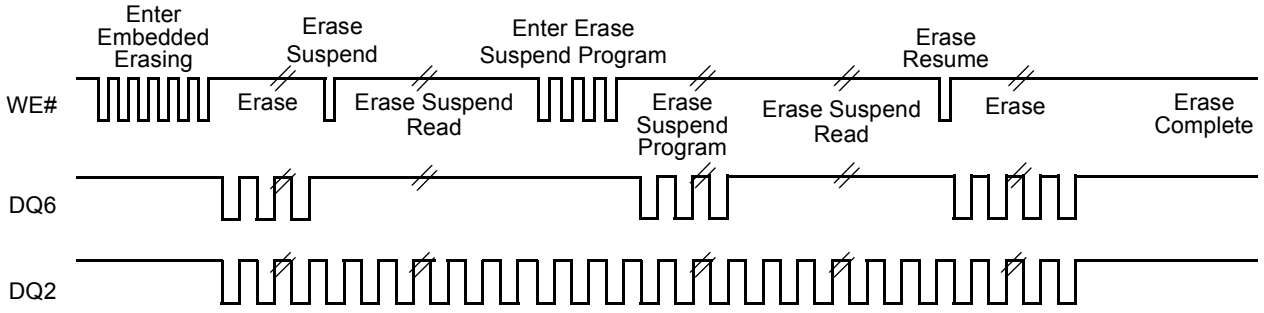
Figure 20. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 21. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 22. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description			Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

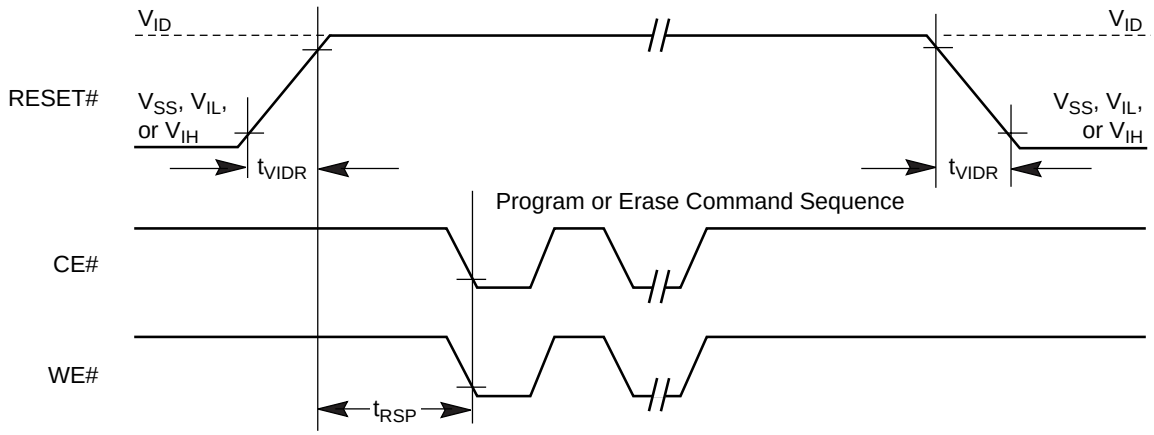
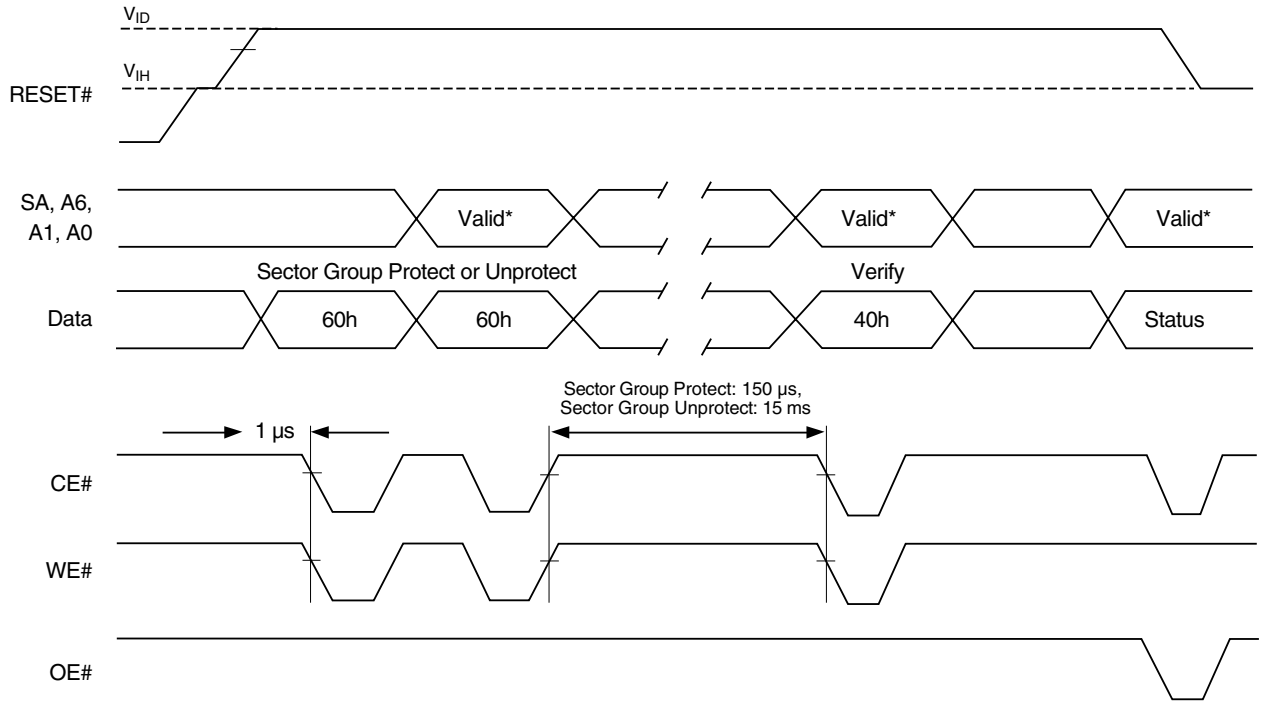


Figure 23. Temporary Sector Group Unprotect Timing Diagram

AC CHARACTERISTICS



* *For sector group protect, A6 = 0, A1 = 1, A0 = 0. For sector group unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 24. Sector Group Protect and Unprotect Timing Diagram

AC CHARACTERISTICS

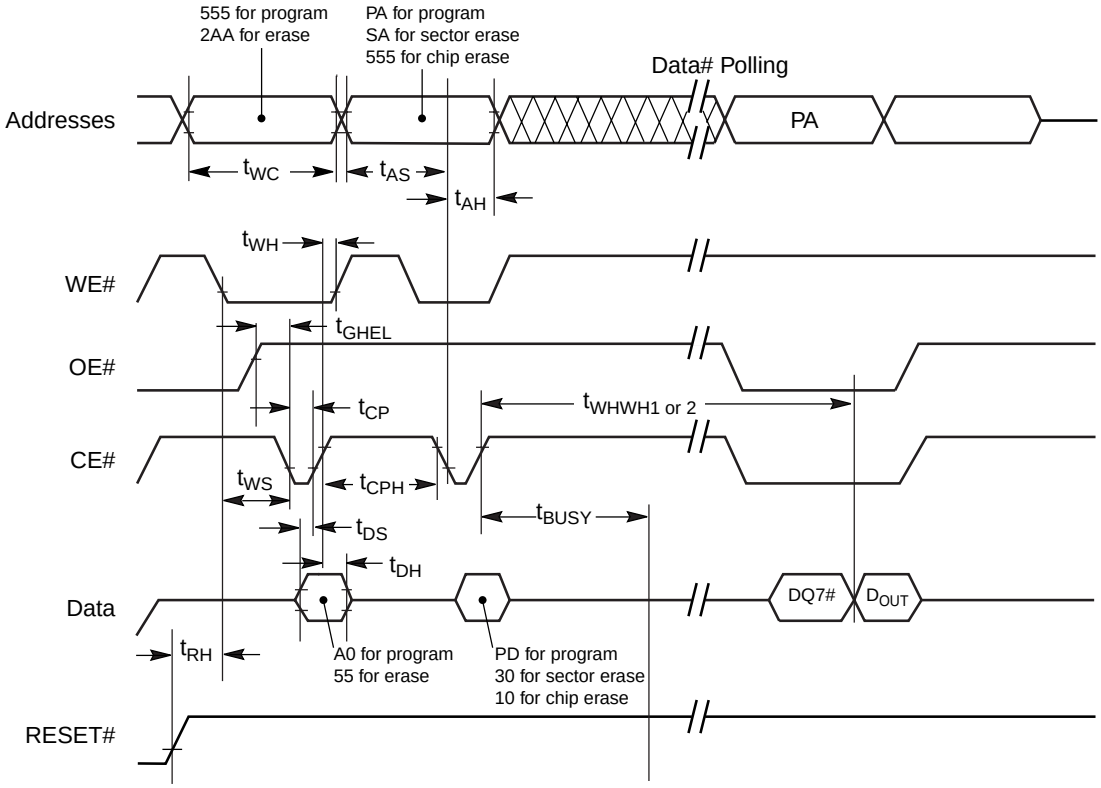
Alternate CE# Controlled Erase and Program Operations

Parameter		Description			15, 11	Unit
JEDEC	Std.					
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	65	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0	ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	45	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30	ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240	µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15	µs
		Effective Accelerated Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	11.8	µs
		Program Operation (Note 2)	Word	Typ	60	µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5	sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*
3. *For 1–16 words.*
4. *Effective write buffer specification is based upon a 16-word write buffer operation.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Waveforms are for the word mode.*

Figure 25. Alternate CE# Controlled Write (Erase/Program) Operation Timings

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	15	sec	Excludes 00h programming prior to erasure (Note 5)
Chip Erase Time		128		sec	
Effective Write Buffer Program Time (Note 3)	Per Word	15	1000	µs	Excludes system level overhead (Note 6)
Program Time	Word	60	1000	µs	
Effective Accelerated Program Time (Note 3)	Word	11.8	785	µs	
Accelerated Program Time	Word	54	900	µs	
Chip Program Time (Note 4)		126		sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 3.0 V, 100,000 cycles.*
3. *Effective write buffer specification is based upon a 16-word write buffer operation.*
4. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
5. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
6. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 10 for further information on command definitions.*
7. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

BGA PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	FBGA	4.2	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	FBGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	FBGA	3.9	4.7	pF

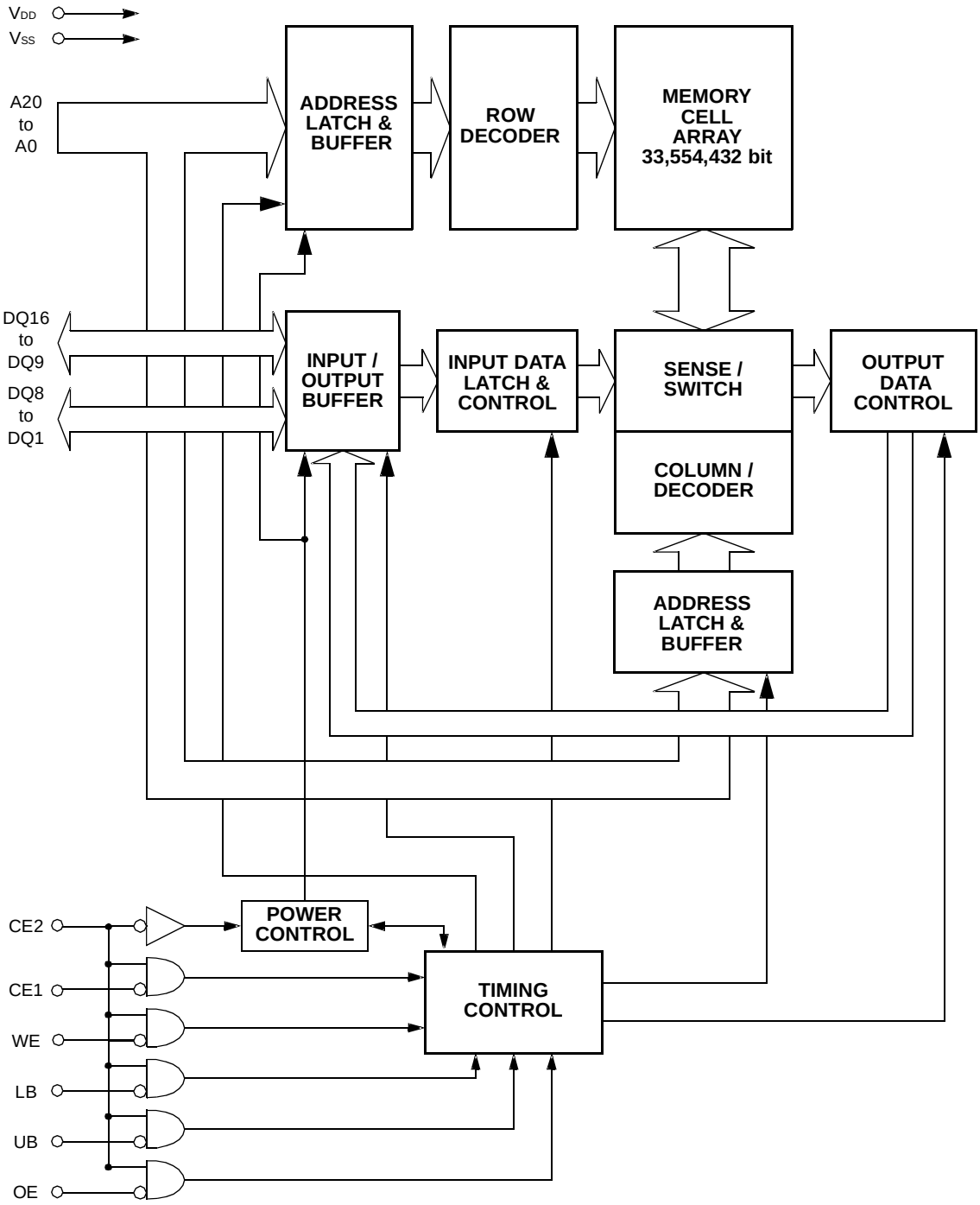
Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PSRAM BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mode	CE2	CE1#	WE#	OE#	LB#	UB#	A20-0	DQ7-0	DQ15-8
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z
Output Disable (Note 1)	H	L	H	H	H	X	(Note 3)	High-Z	High-Z
Output Disable (No Read)			H	L	H	H	Valid	High-Z	High-Z
Read (Upper Byte)					H	L	Valid	High-Z	Output Valid
Read (Lower Byte)					L	H	Valid	Output Valid	High-Z
Read (Word)					L	L	Valid	Output Valid	Output Valid
No Write			L	H (Note 4)	H	H	Valid	Invalid	Invalid
Write (Upper Byte)					H	L	Valid	Invalid	Input Valid
Write (Lower Byte)					L	H	Valid	Input Valid	Invalid
Write (Word)					L	L	Valid	Input Valid	Input Valid
Power Down (Note 2)	L	X	X		X	X	X	High-Z	High-Z

Note:

1. *Should not be kept this logic condition longer than 1 μs.*
2. *Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. Data retention depends on the selection of Power Down Program. Refer to Power down for details.*
3. *Can be either V_{IL} or V_{IH} but must be valid for read or write.*
4. *OE# can be VIL during Write operation if the following conditions are satisfied; Write pulse is initiated by CE1# (refer to CE1# Controlled Write timing), or cycle time of the previous operation cycle is satisfied, OE stays during Write cycle.*

POWER DOWN

Power Down

The Power Down is to enter low power idle state when CE2 stays Low. The pSRAM has two power down modes, Deep Sleep and 8M Partial. These can be programmed by series of read/write operation. See the following table for mode features.

Mode	Data Retention	Retention Address
Sleep (default)	No	N/A
8M Partial	8M bit	00000h to 7FFFFh

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

Power Down Program Sequence

The program requires total 6 read/write operation with unique address and data. Between each read/write operation requires that device be in standby mode. The following table shows the detail sequence.

Cycle#	Operation	Address	Data
1st	Read	1FFFFFh (MSB)	Read Data (RDa)
2nd	Write	1FFFFFh	RDa
3rd	Write	1FFFFFh	RDa
4th	Write	1FFFFFh	Don't Care (X)
5th	Write	1FFFFFh	X
6th	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address (MSB). The second and third cycle are to write back the data (RDa) read by first cycle. If the second or third cycle is written into the different address, the program is cancelled and the data written by the second or third cycle is valid as a normal write operation. The fourth and fifth cycle is to write to MSB. The data of fourth and fifth cycle is don't care. If the fourth or fifth cycle is written into different address, the program is also cancelled but write data may not be wrote as normal write operation. The last cycle is to read from specific address key for mode selection. Once this program sequence is performed from a Partial mode, the write data may be lost. So, it should perform this program prior to regular read/write operation if Partial mode is used.

Address Key

The address key has the following format.

Mode	Address			
	A20	A19	A18-A0	Binary
Sleep (default)	1	1	1	1FFFFFh
8M Partial	1	0	1	17FFFFh

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	2.7	3.1	V
	V_{SS}	0	0	V
High Level Input Voltage	V_{IH}	0.8 V_{DD}	V_{DD} + 0.2 and ≤+3.6	V
	V_{IH}	0.8 V_{DD}	V_{DD} + 0.2	V
Low Level Input Voltage	V_{IL}	-0.3	0.2 V_{DD}	V
Ambient Temperature	T_A	–25	85	°C

Notes:

1. *Maximum DC voltage on input and I/O pins are V_{DD} + 0.2 V. During voltage transitions, inputs may positive overshoot to V_{DD} + 1.0 V for periods of up to 5 ns.*
2. *Minimum DC voltage on input or I/O pins are -0.3 V. During voltage transitions, inputs may negative overshoot V_{SS} to -1.0 V for periods of up to 5 ns.*

PSRAM DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min.	Max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{DD}		-1.0	+1.0	µA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{DD}, Output Disable		-1.0	+1.0	µA
Output High Voltage Level	V_{OH}	$V_{DD} = V_{DD}$(min), I_{OH} = –0.5mA		2.4	–	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1 mA		–	0.4	V
V_{DD} Power Down Current	I_{DDPS}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, CE2 ≤ 0.2V	SLEEP	–	10	µA
	I_{DDP8}		8M Partial	–	50	µA
V_{DD} Standby Current	I_{DDS}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, CE1#		–	1.5	mA
	I_{DDS1}	$V_{DD} = V_{DD}$ max., $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{DD} - 0.2$ V, CE1# =CE2 ≥ VDD – 0.2V		–	80	µA
V_{DD} Active Current	I_{DDA1}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, CE1# = V_{IL} and CE2 = V_{IH}, I_{OUT} = 0 mA	t_{RC}/t_{WC} = minimum	–	30	mA
	I_{DDA2}		t_{RC}/t_{WC} = 1 µs	–	3	mA
V_{DD} Page Read Current	I_{DDA3}	$V_{DD} = V_{DD}$ max., $V_{IN} = V_{IH}$ or V_{IL}, CE1# = V_{IL} and CE2 = V_{IH}, I_{OUT} = 0 mA, t_{PRC} = min.		–	10	mA

Notes:

1. *All voltages are referenced to V_{SS}.*
2. *DC Characteristics are measured after following POWER-UP timing.*
3. *I_{OUT} depends on the output load conditions.*

PSRAM AC CHARACTERISTICS

Read Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
Read Cycle Time (Notes 1, 2)	t_{RC}	65	1000	ns
CE1# Access Time (Note 3)	t_{CE}	–	65	ns
OE# Access Time (Note 3)	t_{OE}	–	40	ns
Address Access Time (Notes 3,5)	t_{AA}	–	65	ns
LB#/UB# Access Time (Note 3)	t_{BA}	–	30	ns
Page Address Access Time (Notes 3,6)	t_{PAA}	–	20	ns
Page Read Cycle Time (Notes 1,6,7)	t_{PRC}	25	1000	ns
Output Data Hold Time (Note 3)	t_{OH}	5	–	ns
CE1# Low to Output Low-Z (Note 4)	t_{CLZ}	5	–	ns
OE# Low to Output Low-Z (Note 4)	t_{OLZ}	0	–	ns
LB#/UB# Low to Output High-Z (Note 4)	t_{BLZ}	0	–	ns
CE1# High to Output High-Z (Note 3)	t_{CHZ}	–	20	ns
OE# High to Output High-Z (Note 3)	t_{OHZ}	–	20	ns
LB#/UB# High to Output High-Z (Note 3)	t_{BHZ}	–	20	ns
Address Setup Time to CE1# Low	t_{ASC}	-5	–	ns
Address Setup Time to OE# Low	t_{ASO}	10	–	ns
Address Invalid Time (Notes 5,8)	t_{AX}	–		ns
Address Hold Time from CE1# High (Note 9)	t_{CHAH}	-5	–	ns
Address Hold Time from OE# High	t_{OHAH}	-5	–	ns
CE1# High Pulse Width	t_{CP}	12	–	ns

Notes:

1. *Maximum value is applicable if CE1# is kept at Low without change of address input of A3 to A20.*
2. *Address should not be changed within minimum t_{RC}.*
3. *The output load 50pF.*
4. *The output load 5pF.*
5. *Applicable to A3 to A20 when CE1# is kept at Low.*
6. *Applicable only to A0, A1 and A2 when CE1# is kept at Low for the page address access.*
7. *In case Page Read Cycle is continued with keeping CE1# stays Low, CE1# must be brought to High within 4 μs. In other words, Page Read Cycle must be closed within 4 μs.*
8. *Applicable when at least two of address inputs among applicable are switched from previous state.*
9. *t_{RC} (min) and t_{PRC} (min) must be satisfied.*

PSRAM AC CHARACTERISTICS

Write Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
Write Cycle Time (Notes 1, 2)	t_{WC}	65	1000	ns
Address Setup Time (Note 3)	t_{AS}	0	–	ns
CE1# Write Pulse Width (Note 3)	t_{CW}	40	–	ns
WE# Write Pulse Width (Note 3)	t_{WP}	40	–	ns
LB#/UB# Write Pulse Width (Note 3)	t_{BW}	40	–	ns
LB#/UB# Byte Mask Setup Time (Note 4)	t_{BS}	-5	–	ns
LB#/UB# Byte Mask Hold Time (Note 5)	t_{BH}	-5	–	ns
CE1# Write Recovery Time (Note 6)	t_{WRC}	12	–	ns
WE# Write Recovery Time (Note 6)	t_{WR}	7.5	1000	ns
LB#/UB# Write Recovery Time (Note 6)	t_{BR}	12	1000	ns
Data Setup Time	t_{DS}	12	–	ns
Data Hold Time	t_{DH}	0	–	ns
OE# High to CE1# Low Setup Time for Write (Note 7)	t_{OHCL}	-5	–	ns
OE# High to Address Setup Time for Write (Note 8)	t_{OES}	0	–	ns
WE#/UB#/LB# High to OE# Low Setup Time for Read (Note 10)	t_{WHOL}	12	–	10
LB# and UB# Write Pulse Overlap	t_{BWO}	30	–	ns
CE1# High Pulse Width	t_{CP}	12	–	ns
Address Hold Time for Write End (Note 3)	t_{AH}	0	–	ns

Notes:

1. *Maximum value is applicable if CE1# is kept at Low without any address change.*
2. *Minimum value must be equal or greater than the sum of write pulse (t_{CW}, T_{WP}, T_{BW}) and write recovery time (t_{WCR}, T_{WR} or t_{BR}).*
3. *Write pulse is defined from High to Low transition of CE1#, WE#, or LB#/UB#, whichever occurs last.*
4. *Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of CE1# or WE# whichever occurs last.*
5. *Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of CE1# or WE# whichever occurs first.*
6. *Write recovery is defined from Low to High transition of CE1#, WE#, or LB#/UB#, whichever occurs first.*
7. *If OE# is Low after minimum t_{OHCL}, read cycle is initiated. In other words, OE# must be brought to High within 5 ns after CE1# is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met*
8. *If OE# is Low after new address input, read cycle is initiated. In other words, OE# must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met and data bus is in High-Z*
9. *Absolute minimum values and defined at minimum V_{IH} level.*
10. *If the actual value of t_{WHOL} is shorter than the specified minimum values, the actual t_{AA} of following Read may become longer by the amount of subtracting the actual value from the specified minimum value.*

AC CHARACTERISTICS

Power Down Parameters

Parameter	Symbol	Value		Unit
		Min.	Max.	
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	–	ns
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	65	–	ns
CE1# High Hold Time following CE2 High after Power Down Exit (SLEEP mode only) (Note 1)	t_{CHH}	300	–	µs
CE1# High Hold Time following CE2 High after Power Down Exit (not in SLEEP mode) (Note 2)	t_{CHHP}	1	–	µs
CE1# High Setup Time following CE2 High after Power Down Exit (Note 1)	t_{CHS}	0	–	ns

Notes:

1. *Applicable also to power up.*
2. *Applicable when 8M Partial mode is programmed.*

Other Timing Parameters

Parameter	Symbol	Value		Unit
		Min.	Max.	
CE#1 High to OE# Invalid Time for Standby Entry	t_{CHOX}	10	-	ns
CE#1 High to WE# Invalid Time for Standby Entry (Note 1)	t_{CHWX}	10	-	ns
CE2 Low Hold Time after Power up	t_{C2LH}	50	–	µs
CE1# High Hold Time following CE2 High after Power up	t_{CHH}	300	–	µs
Input Transition Time (Note 2)	t_T	1	25	ns

Notes:

1. *Some data might be written into any address location if t_{CHWX} (min) is not satisfied*
2. *The Input Transition Time (t_T) at AC testing is 5ns, as shown in AC Test Conditions below... If actual t_T is longer than 5ns, it may violate AC specification of some timing parameters.*

AC CHARACTERISTICS

AC Test Conditions

Symbol	Description	Test Setup	15, 11	Unit
V_{IH}	Input High Level		V_{DD} * 0.8	V
V_{IL}	Input Low Level		V_{DD} * 0.2	V
V_{REF}	Input Timing Measurement Level		V_{DD} * 0.5	V
t_T	Input Transition Time	Between V_{IL} and V_{IH}	5	ns

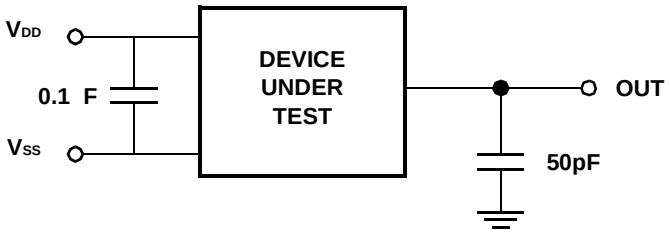
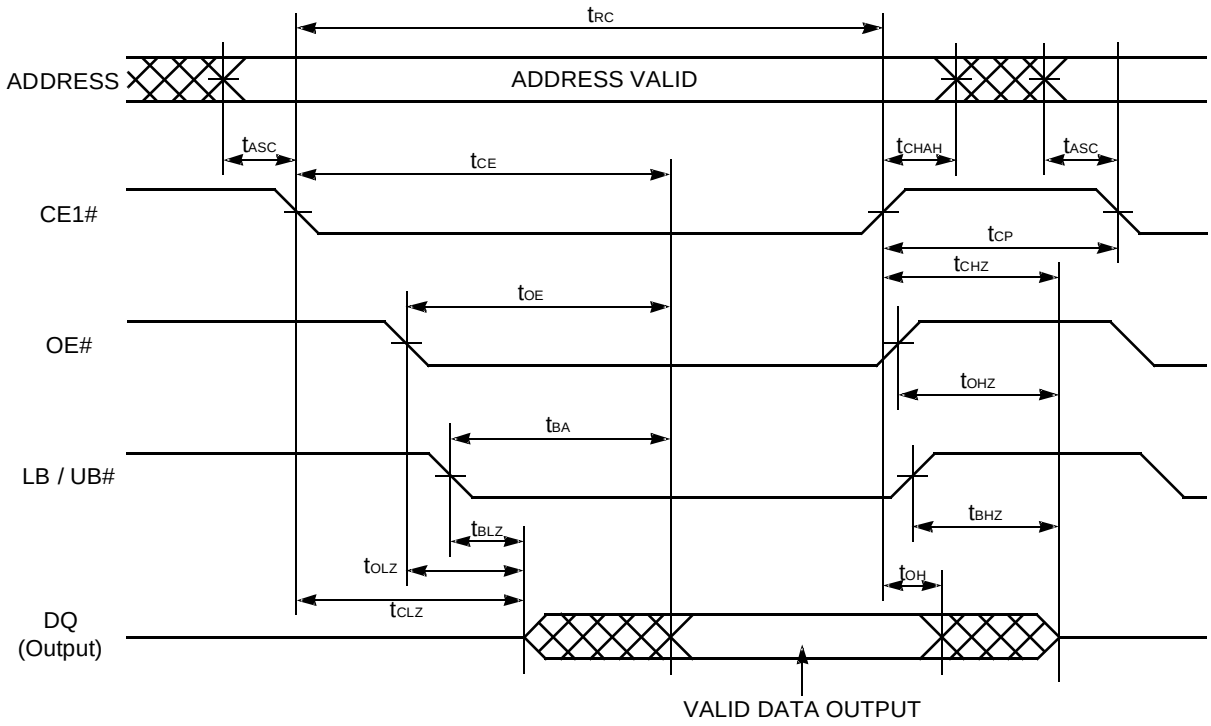


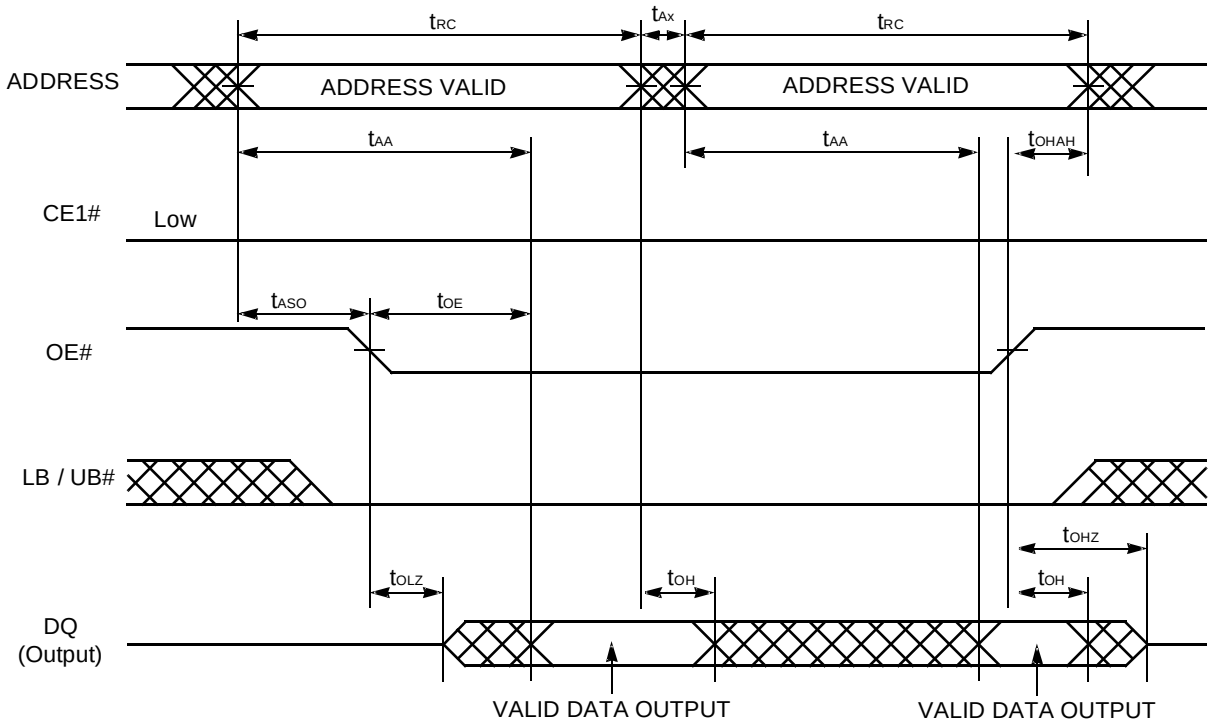
Figure 26. AC Measurement Output Load Circuit

TIMING DIAGRAMS



Note: *CE2 and WE# must be High for entire read cycle.*

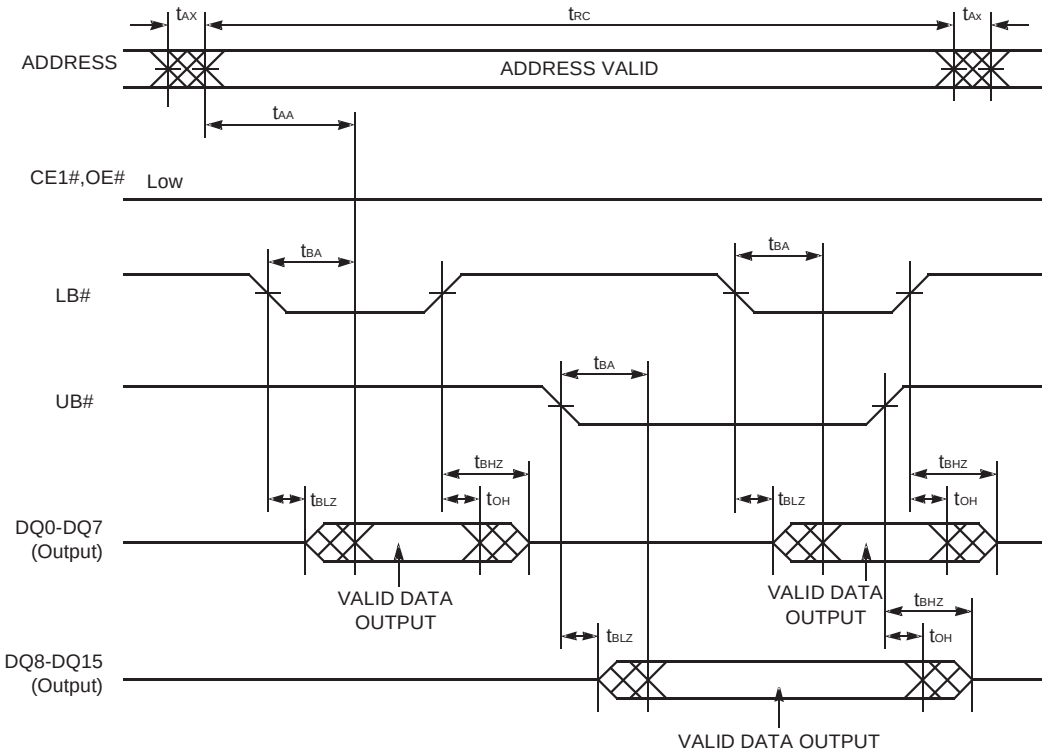
Figure 27. Read TIming #1 (Basic Timing)



Note: *CE2 and WE# must be High for entire read cycle.*

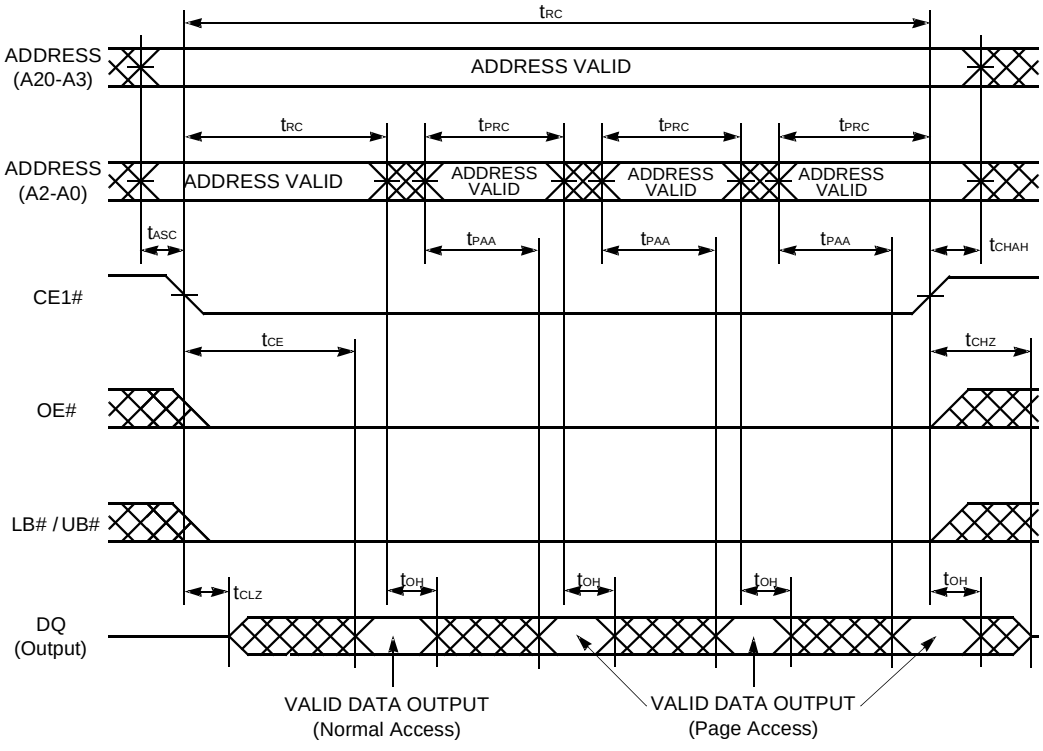
Figure 28. Read Timing #2 (OE# and Address Access)

TIMING DIAGRAMS



Note: *CE2 and WE# must be High for entire read cycle.*

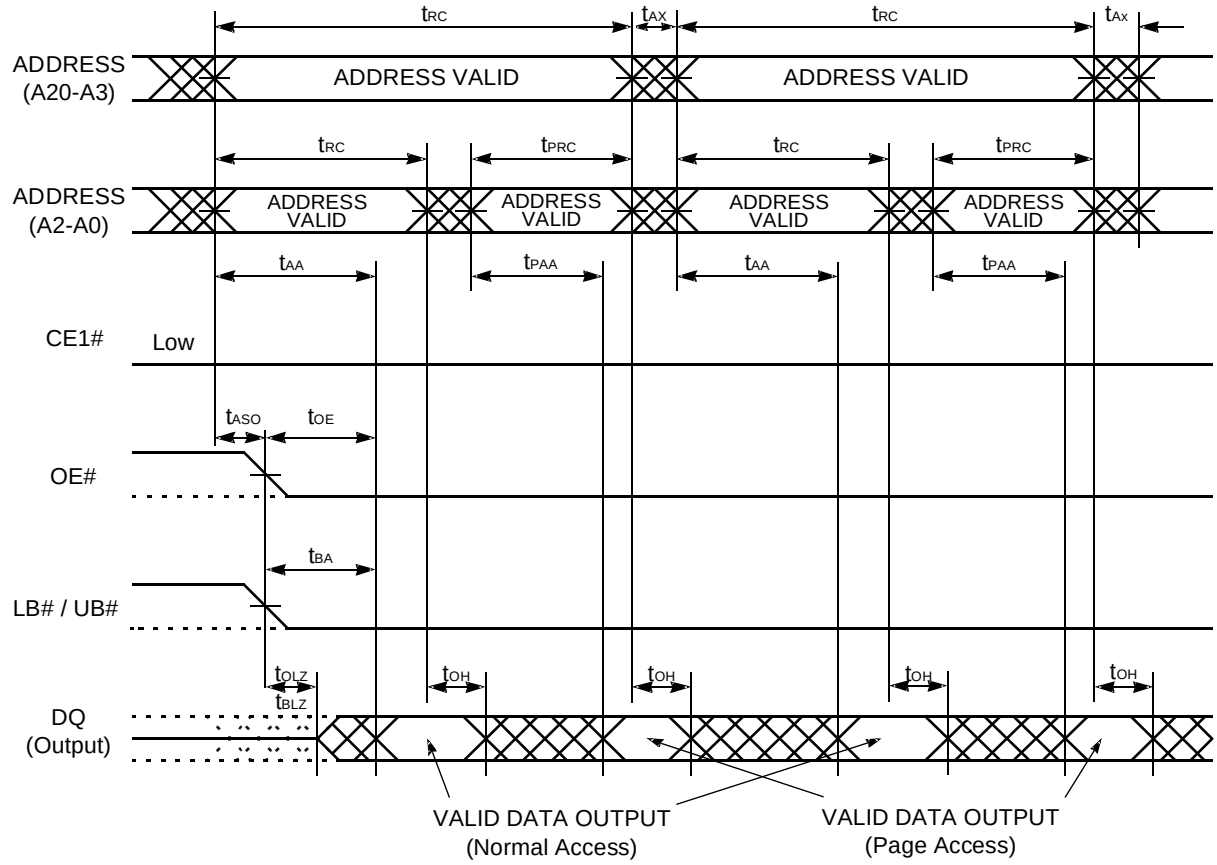
Figure 29. Read Timing #3 (LB#/UB# Byte Access)



Note:*CE2 and WE# must be High for entire read cycle.*

Figure 30. Read Timing #4 (Page Access after CE1# Control Access)

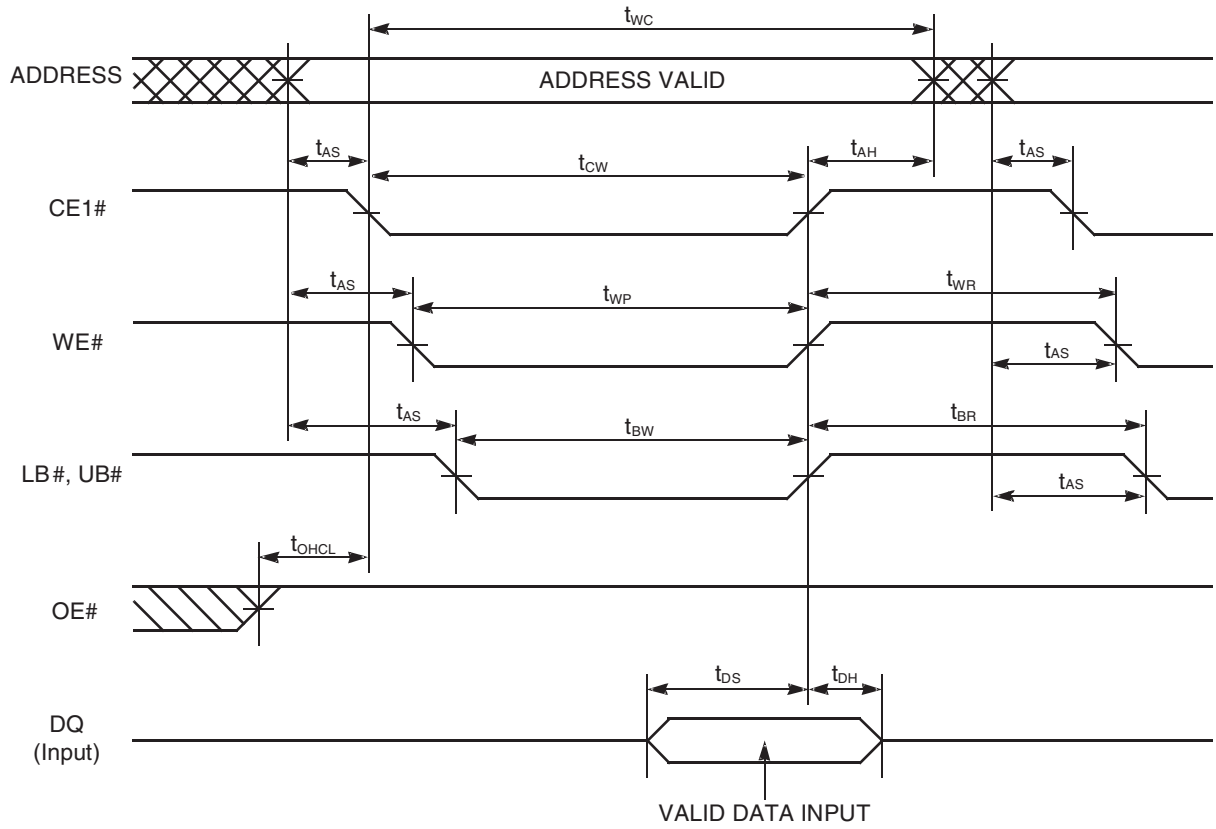
TIMING DIAGRAMS



Note: *CE2 and WE# must be High for entire read cycle. Either or both LB# and UB# must be Low when both CE1# and OE# are Low.*

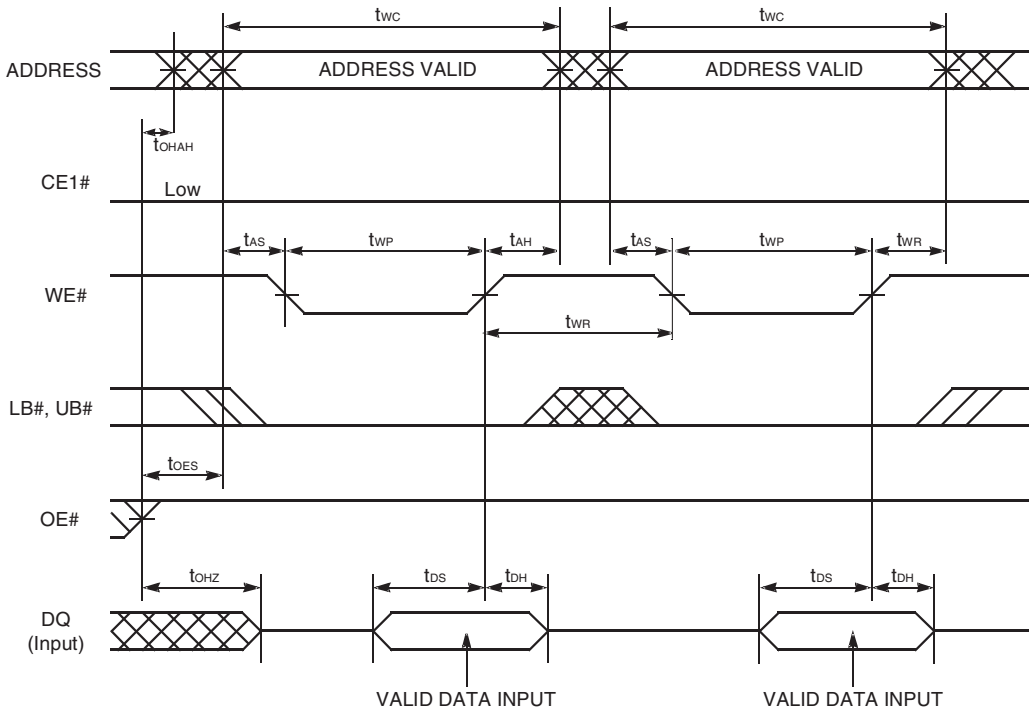
Figure 31. Read Timing #5 (Random and Page Address Access)

TIMING DIAGRAMS



Note: *CE2 must be High for Write Cycle.*

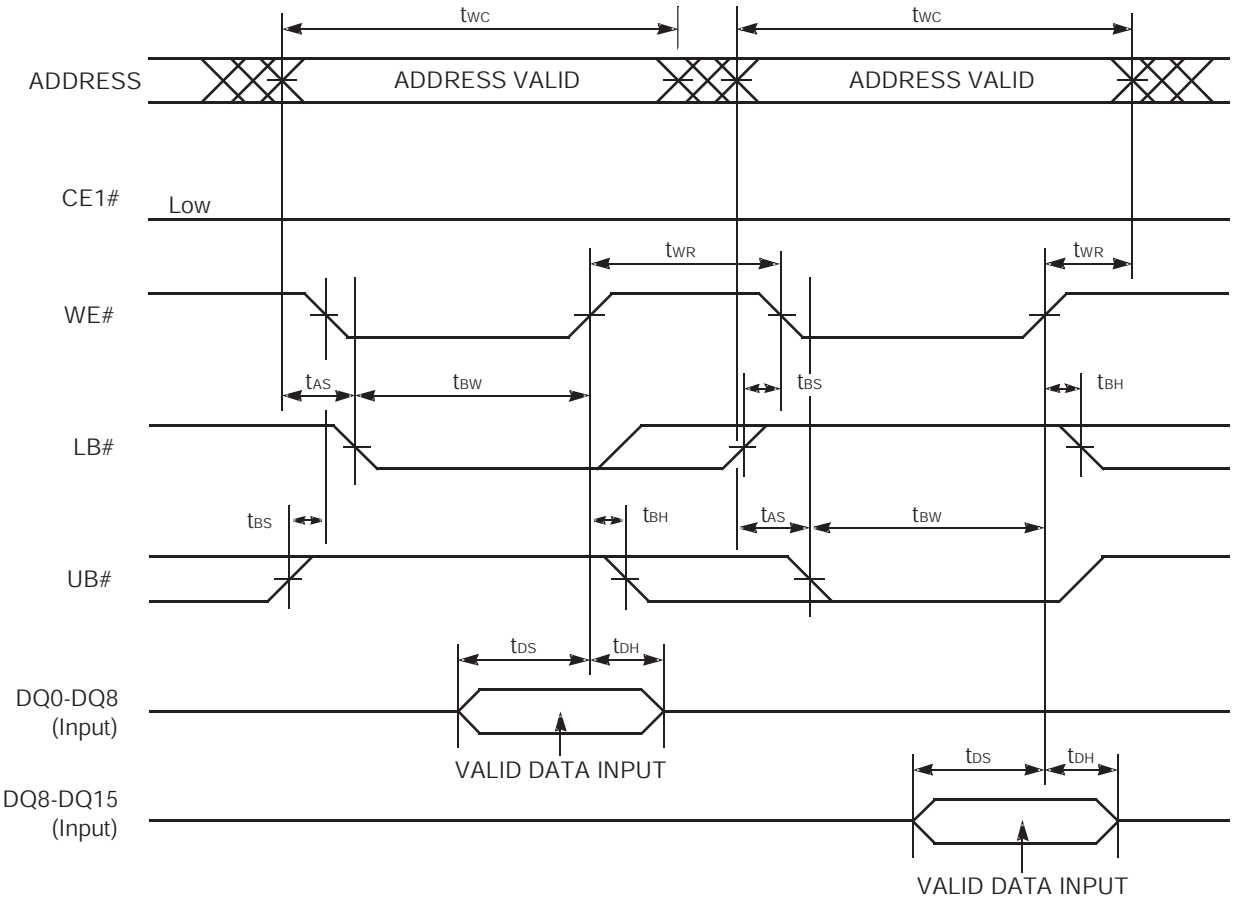
Figure 32. Write Timing #1 (Basic Timing)



Note: *CE2 must be High for Write Cycle.*

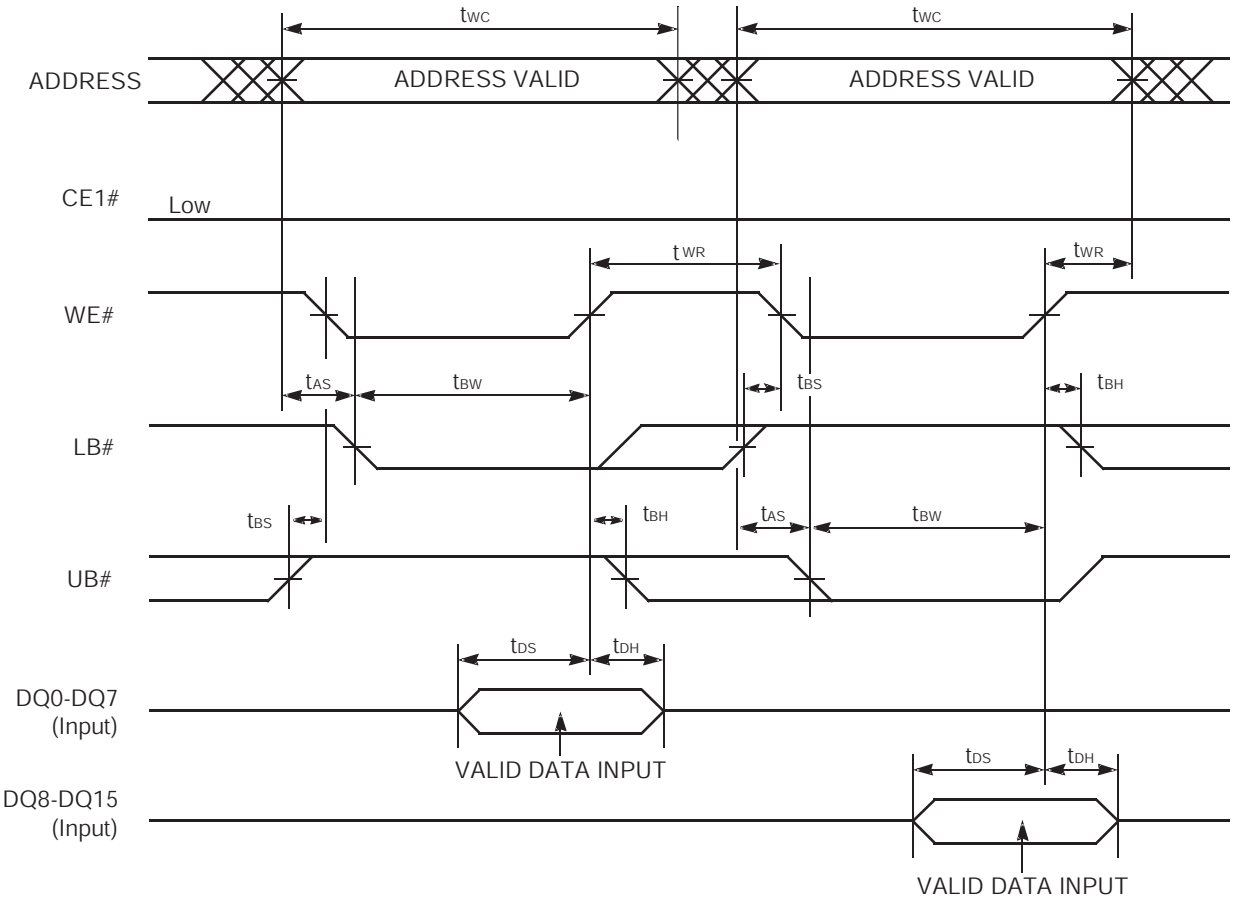
Figure 33. Write Timing #2 (WE# Control)

TIMING DIAGRAMS



Note: *CE2 must be High for Write Cycle.*

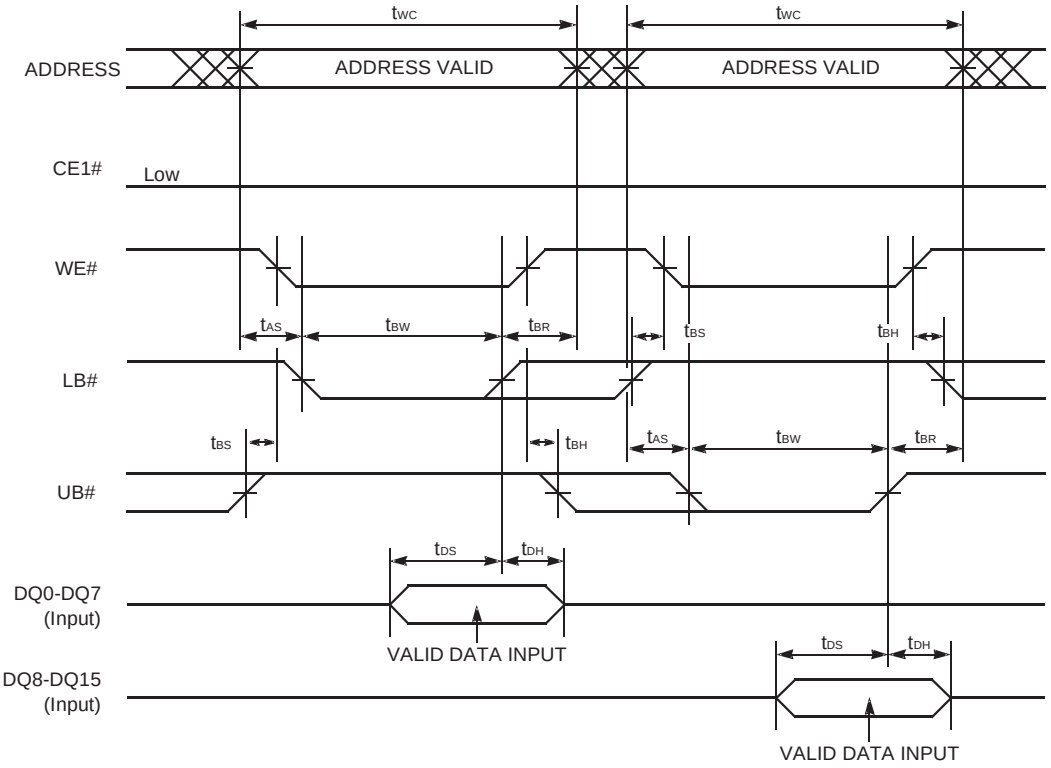
Figure 34. Write Timing #3-1 (WE#/LB#/UB# Byte Write Control)



Note: *CE2 must be High for Write Cycle.*

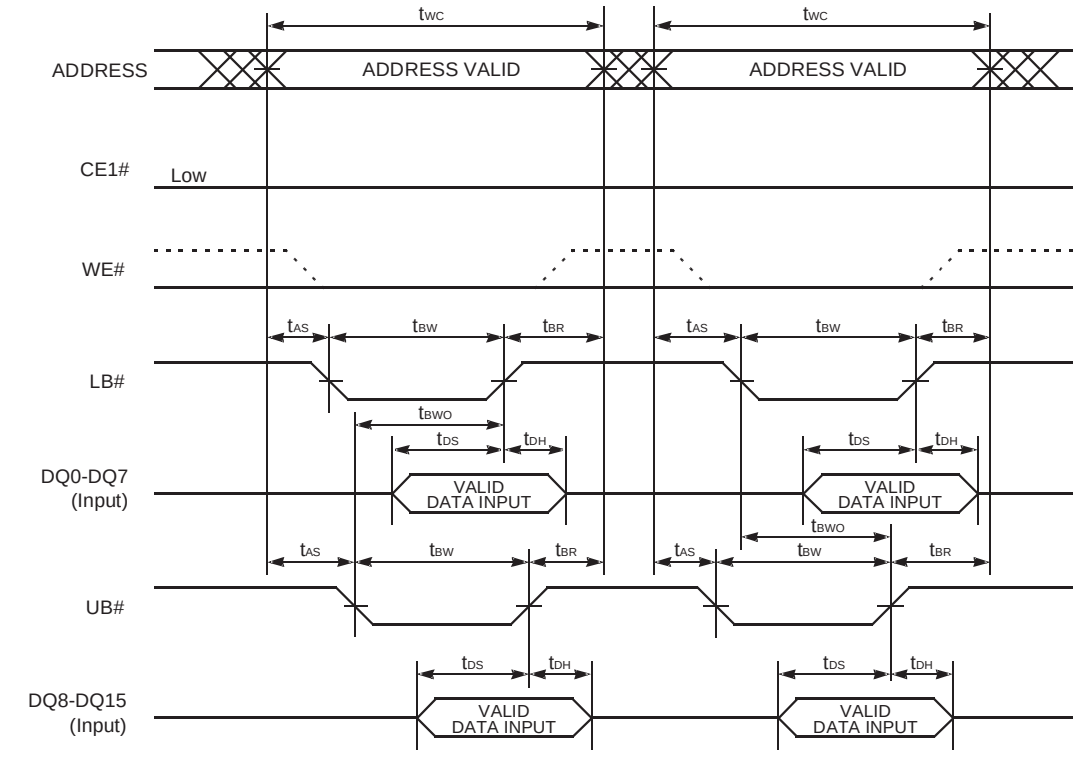
Figure 35. Write Timing #3-2 (WE#/LB#/UB# Byte Write Control)

TIMING DIAGRAMS



Note: *CE2 must be High for Write Cycle.*

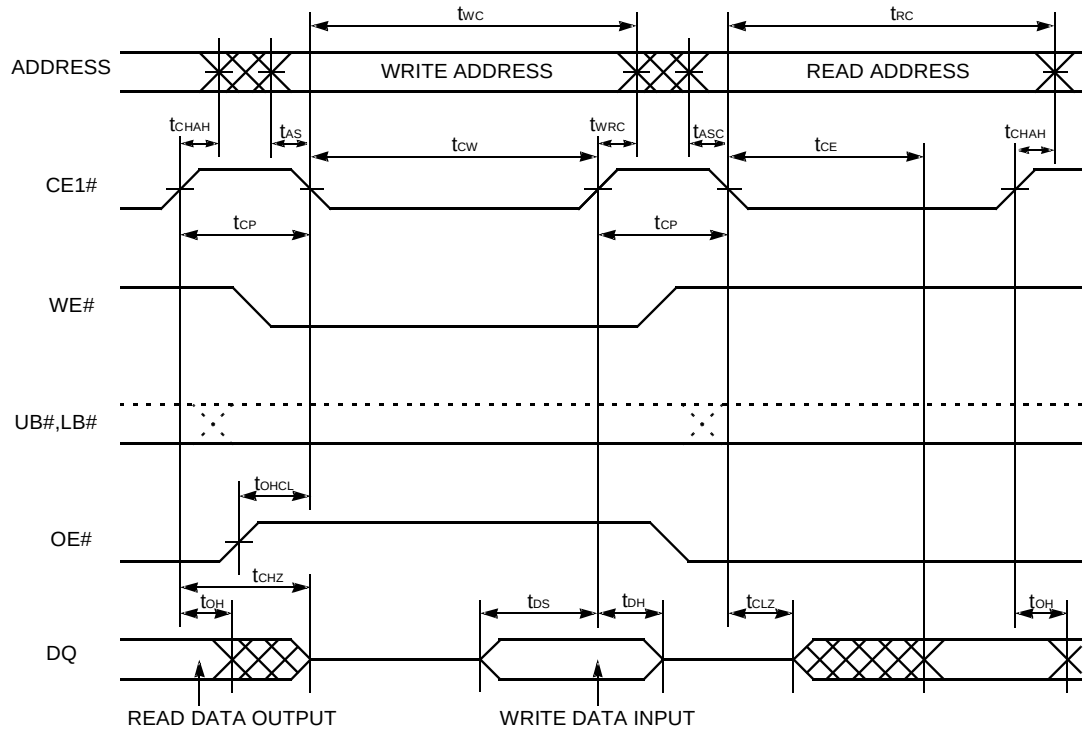
Figure 36. Write Timing #3-3 (WE#/LB#/UB# Byte Write Control)



Note: *CE2 must be High for Write Cycle.*

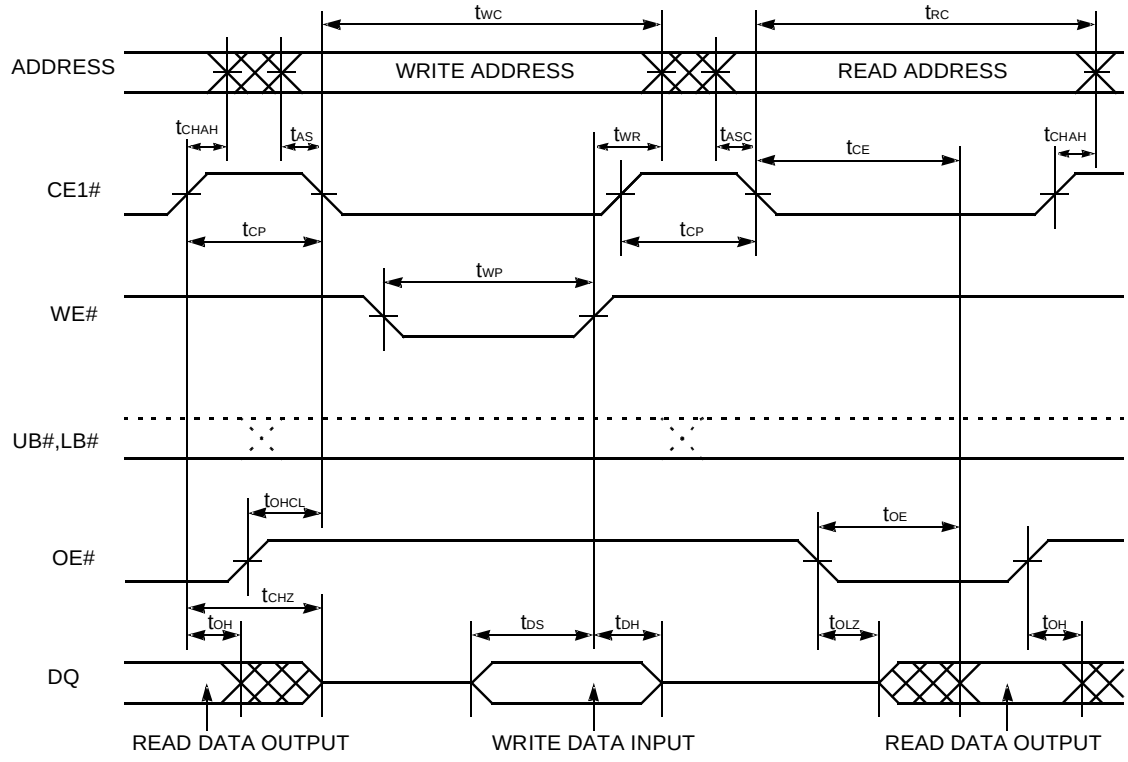
Figure 37. Write Timing #3-4 (WE#/LB#/UB# Byte Write Control)

TIMING DIAGRAMS



Note: *Write address is valid from either CE1# or WE# of last falling edge.*

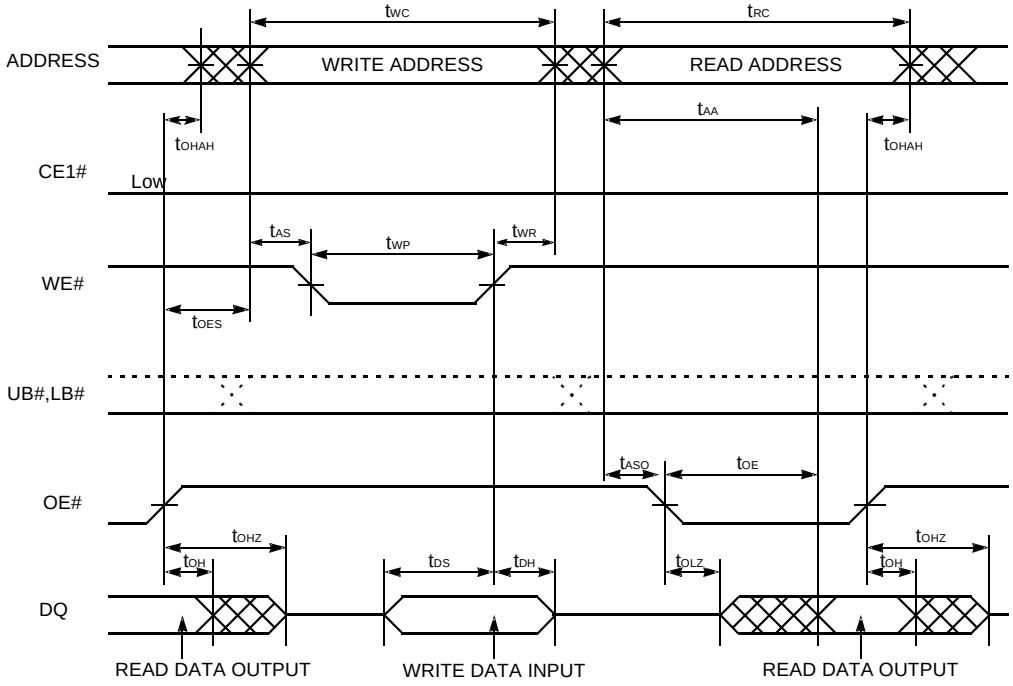
Figure 38. Read/Write Timing #1-1 (CE1# Control)



Note: *OE# can be fixed Low during write operation if it is CE1# controlled write at Read-Write-Read sequence.*

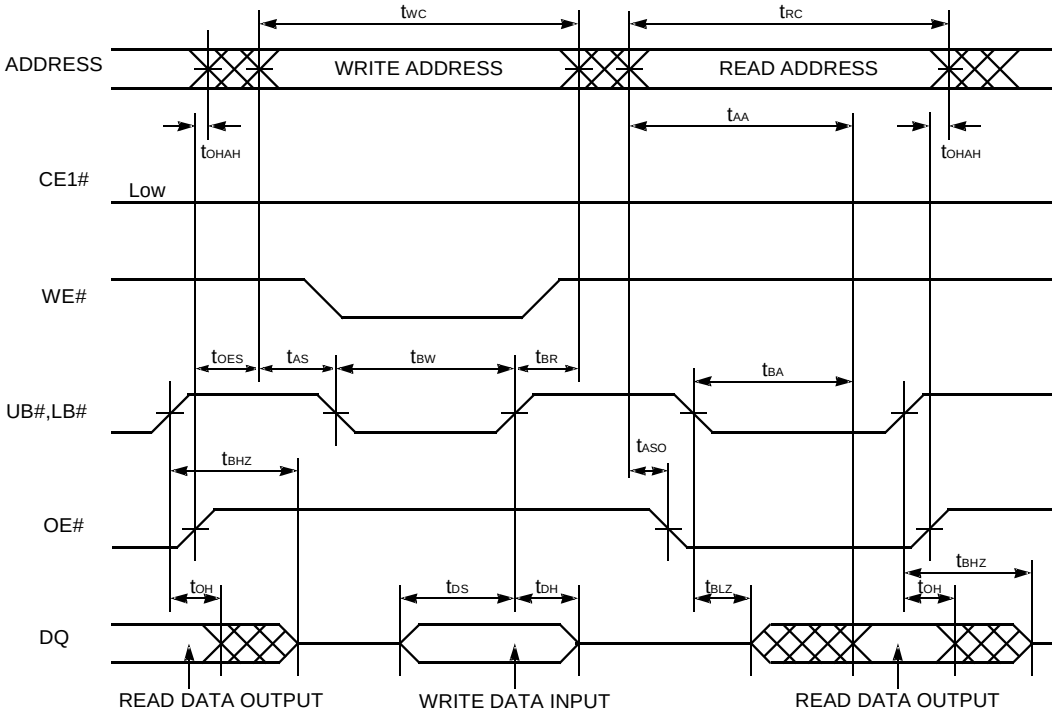
Figure 39. Read/Write Timing #1-2 (CE1#/WE#/OE# Control)

TIMING DIAGRAMS



Note: *CE1# can be tied to Low for WE# and OE# controlled operation.*

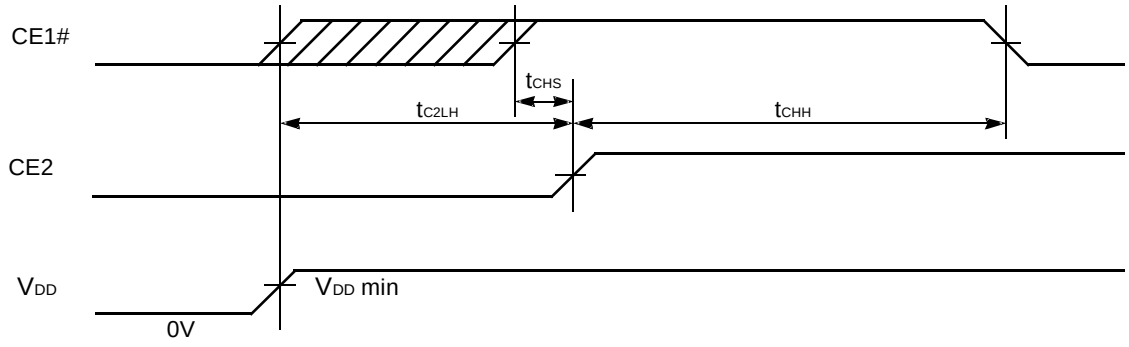
Figure 40. Read/Write Timing #2 (OE#, WE# Control)



Note: *CE#1 can be tied to Low for WE# and OE# controlled operation.*

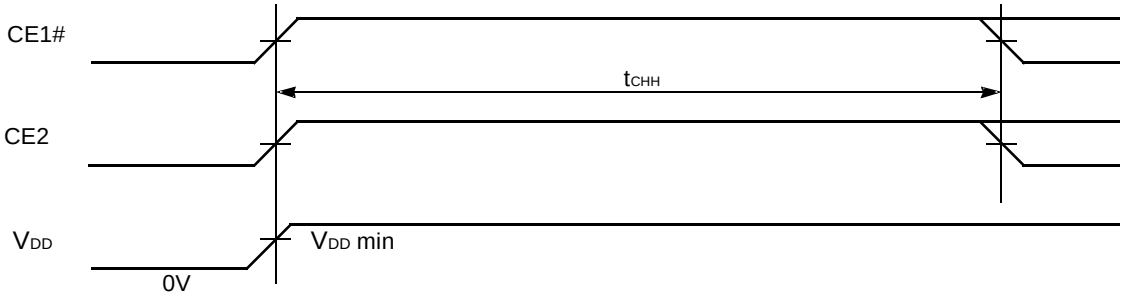
Figure 41. Read/Write Timing #3 (OE#, WE#, LB#, UB# Control)

TIMING DIAGRAMS



Note: *The t_{C2LH} specifies after V_{DD} reaches specified minimum level.*

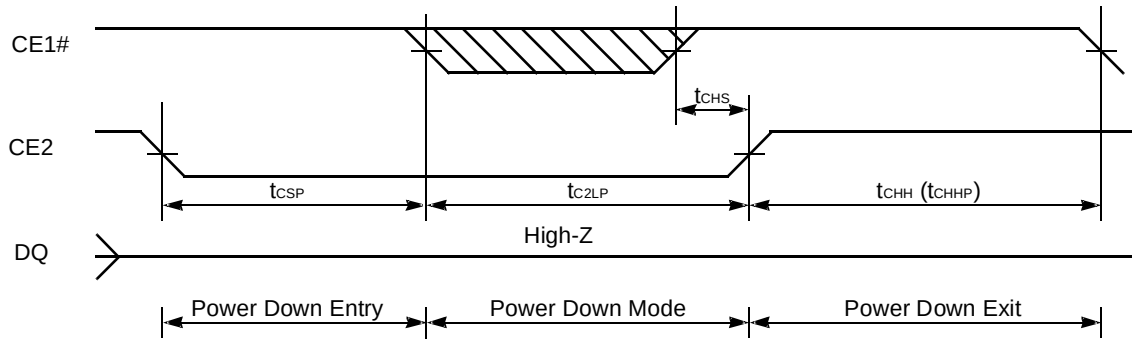
Figure 42. Power-up Timing #1



Note: *The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both CE1# and CE2.*

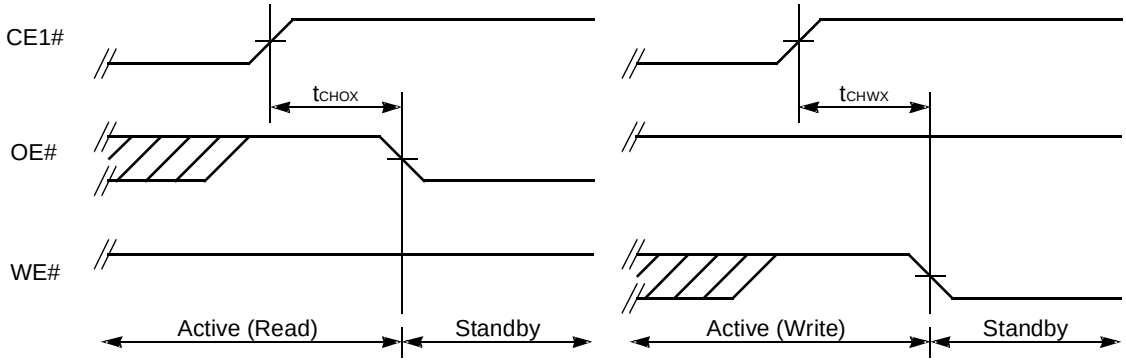
Figure 43. Power-up Timing #2

TIMING DIAGRAMS



Note: *This Power Down mode can be also used as a reset timing if Power-up timing above could not be satisfied and Power-Down program was not performed prior to this reset.*

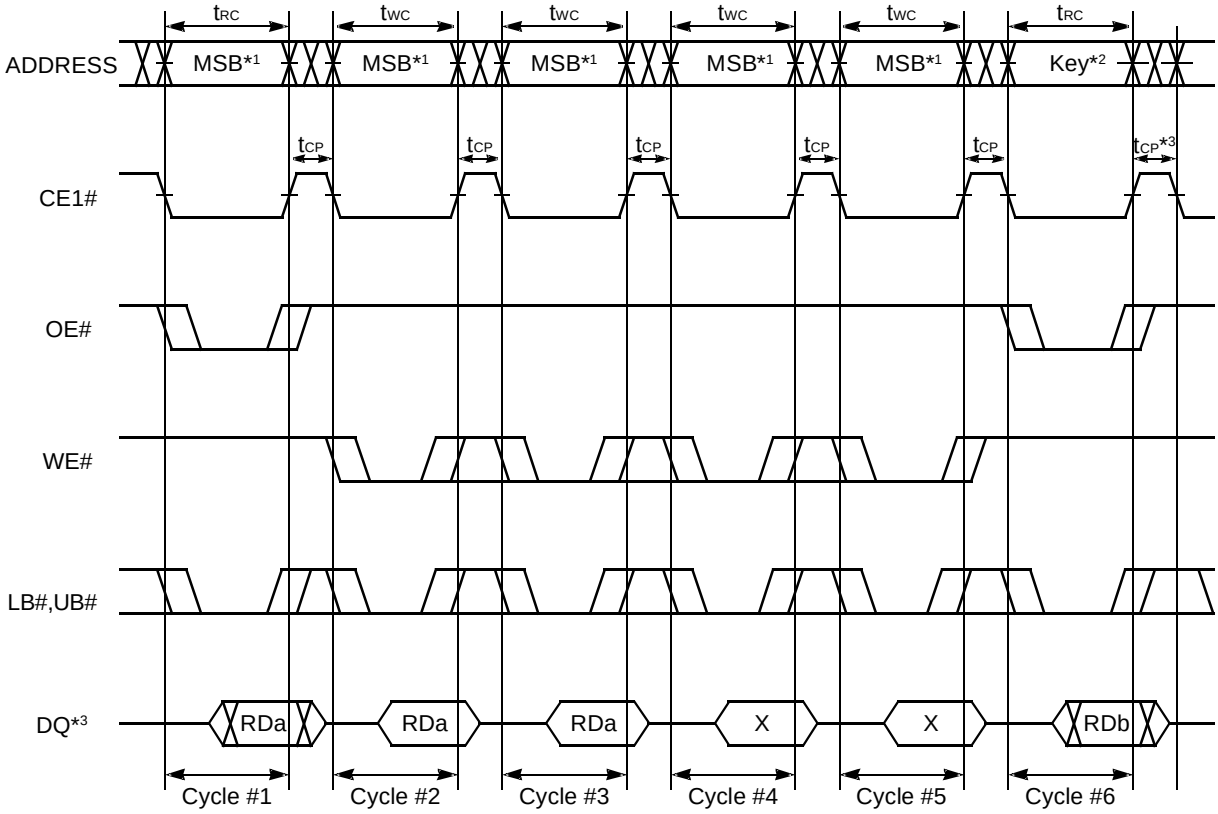
Figure 44. Power-down Entry and Exit Timing



Note: *Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period for standby mode from CE1# Low to High transition.*

Figure 45. Standby Entry Timing after Read or Write

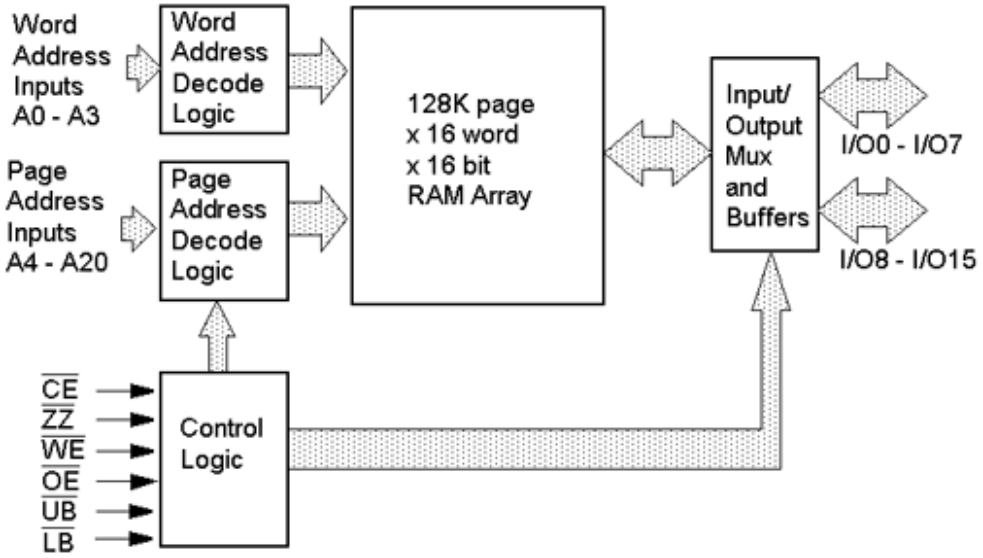
TIMING DIAGRAMS



Notes:

1. *The all address inputs must be High from Cycle #1 to #5.*
2. *After t_{CP} following Cycle #6, the Power Down Program is completed and returned to the normal operation.*

PSRAM BLOCK DIAGRAM



Note: ZZ# = CE2pS on MCP pin-out.

FUNCTION TRUTH TABLE

Mode	CE#	ZZ#	WE#	OE#	UB#	LB#	I/O_0 - I/O_{15} (Note1)	POWER
Standby (Note 2)	H	H	X	X	X	X	High-Z	Standby
Standby (Note 2)	X	H	X	X	H	H	High-Z	Standby
Write	L	H	L	X (Note 3)	L (Note 1)	L (Note 1)	Data In	Active
Read	L	H	H	L	L (Note 1)	L (Note 1)	Data Out	Active
Active	L	H	H	H	L	L	High-Z	Active
Deep Sleep	X	L	X	X	X	X	High-Z	Deep Sleep

Note:

1. *When UB# and LB# are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When LB# only is in the select mode only I/O_0 - I/O_7 are affected as shown. When UB# is in the select mode only I/O_8 - I/O_{15} are affected as shown.*
2. *When the device is in standby mode, control inputs (WE#, OE#, UB#, and LB#), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.*
3. *When WE# is invoked, the OE# input is internally disabled and has no effect on the circuit.*

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.2 to V_{CC}+0.3	V
Voltage on VCC Supply Relative to V_{SS}	V_{CC}	–0.2 to 3.6	V
Power Dissipation	P_D	1	W
Storage Temperature	T_{STG}	–40 to 125	°C
Operating Temperature	T_A	-25 to +85	°C

Note:

1. *Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

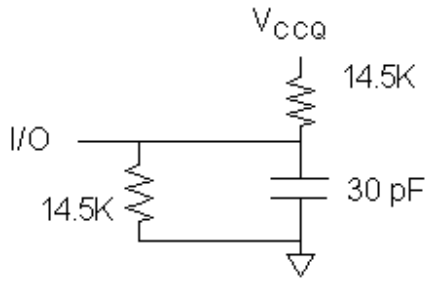
OPERATING CHARACTERISTICS (OVER SPECIFIED TEMPERATURE RANGE)

Item	Symbol	Test Condition	Min	Typ (Note 1)	Max	Unit
Supply Voltage	V_{CC}		2.7	3.0	3.1	V
Supply Voltage for I/O	V_{CCQ}		2.7	3.0	V_{CC}	V
Input High Voltage	V_{IH}		$0.8V_{CCQ}$		V_{CCQ}+0.2	V
Input Low Voltage	V_{IL}		-0.2		$0.2V_{CCQ}$	V
Output High Voltage	V_{OH}	I_{OH} = 0.5mA	$0.8V_{CCQ}$			V
Output Low Voltage	V_{OL}	I_{OL} = -0.5mA			$0.2V_{CCQ}$	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	-1		1	µA
Output Leakage Current	I_{LO}	OE# = V_{IH} or Chip Disabled	-1		1	µA
Read/Write Operating Supply Current @1 µs Cycle Time (Note 2)	I_{CC1}	V_{CC}= 3.1V, V_{IN}=CMOS levelsChip Enabled, I_{OUT} = 0			3.0	mA
Read/Write Operating Supply Current @65 ns Cycle Time (Note 2)	I_{CC2}	V_{CC}= 3.1V, V_{IN}=CMOS levels Chip Enabled, I_{OUT} = 0			25.0	mA
Page Mode Operating Supply Current @65 ns Cycle Time (Note 2)	I_{CC2}	V_{CC}= 3.1V, V_{IN}=CMOS levels Chip Enabled, I_{OUT} = 0			25.0	mA
Maximum Standby Current (Note 3)	I_{SB1}	V_{CC}= 3.1V, V_{IN}=CMOS levels Chip Disabled		80	120	µA

Note:

1. *Typical values are measured at Vcc=Vcc Typ., TA=25°C and not 100% tested.*
2. *This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.*
3. *This device assumes a standby mode if the chip is disabled (either CE# high or both UB# and LB# high). In order to achieve low standby current all inputs must be within 0.2V of either VCC or VSS.*

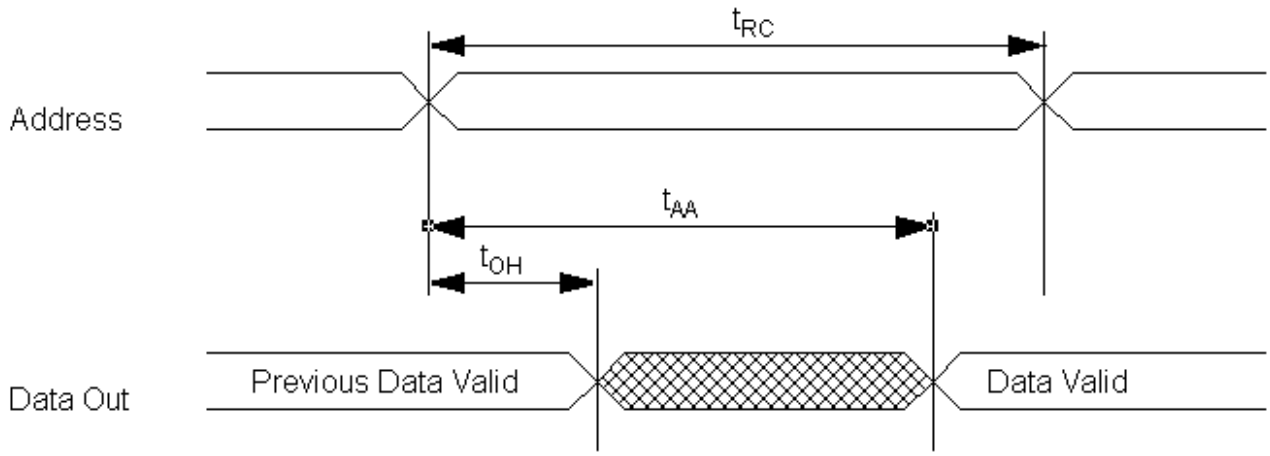
OUTPUT LOAD CIRCUIT



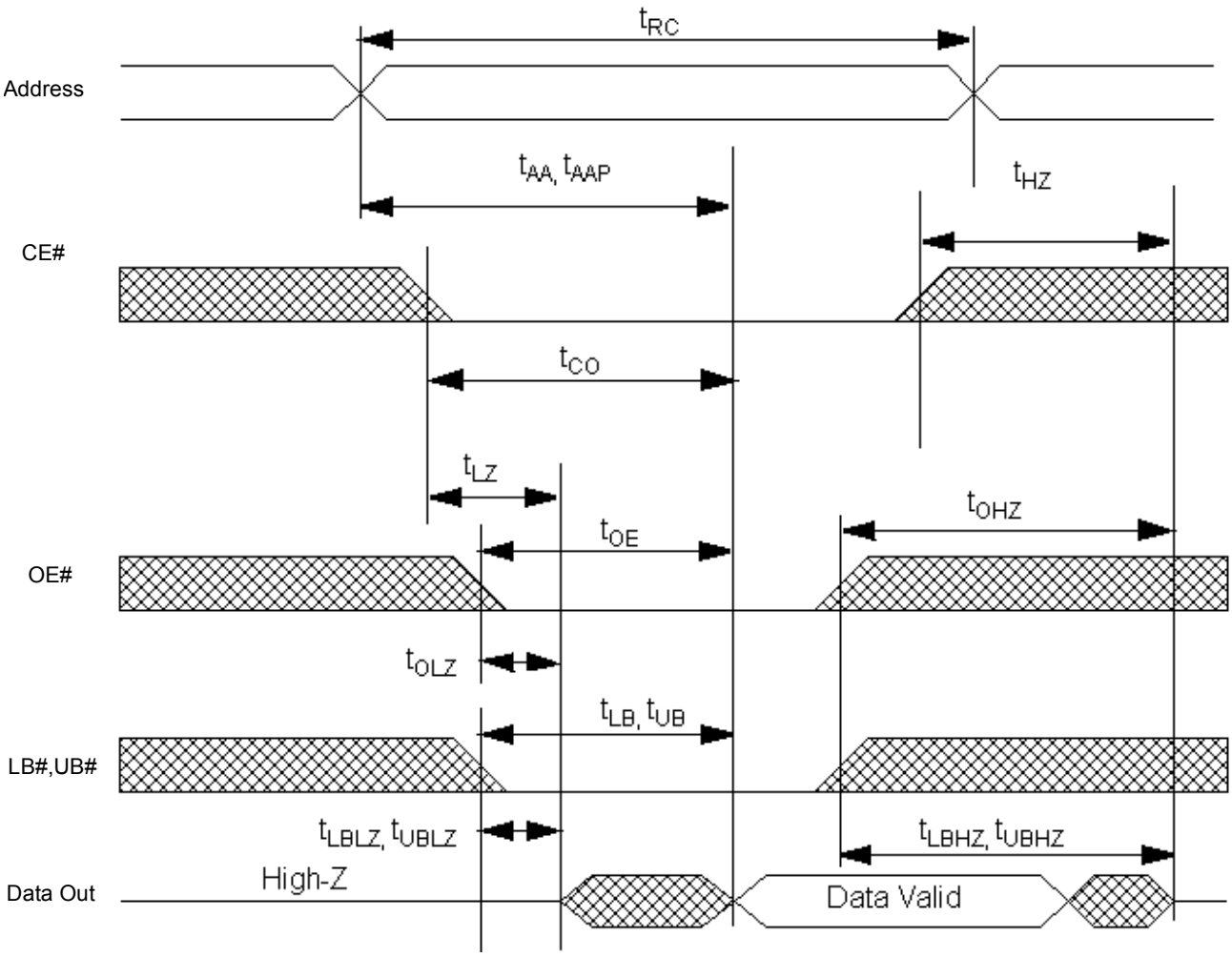
TIMING

Item	Symbol	65ns		Units
		Min.	Max.	
Read Cycle Time	t_{RC}	65		ns
Address Access Time	t_{AA}		65	ns
Page Mode Read Cycle Time	t_{PC}	25	20000	ns
Page Mode Access Time	t_{PA}		25	ns
Chip Enable to Valid Output	t_{CO}		65	ns
Output Enable to Valid Output	t_{OE}		20	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		65	ns
Chip Enable to Low-Z Output	t_{LZ}	10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	10		ns
Chip Disable to High-Z Output	t_{HZ}	0	5	ns
Output Disable to High-Z Output	t_{OHZ}	0	5	ns
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	0	5	ns
Output Hold from Address Change	t_{OH}	5		ns
Write Cycle Time	t_{WC}	65		ns
Page Mode Write Cycle Time	t_{PWC}	25	20000	ns
Page Mode CE Precharge	t_{CP}	10		ns
Chip Enable to End of Write	t_{CW}	55		ns
Address Valid to End of Write	t_{AW}	55		ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	55		ns
Write Pulse Width	t_{WP}	50	20000	ns
Write Precharge Time	t_{WEH}	7.5		ns
Address Setup Time	t_{AS}	0		ns
Write Recovery Time	t_{WR}	0		ns
Write to High-Z Output	t_{WHZ}		5	ns
Data to Write Time Overlap	t_{DW}	25		ns
Page Mode Data to Write Time Overlap	t_{PDW}	20		ns
Data Hold from Write Time	t_{DH}	0		ns
Page Mode Data Hold from Write Time	t_{PDH}	0		ns
End Write to Low-Z Output	t_{OW}	5		ns
Maximum Page Mode Cycle	t_{PGMAX}		20000	ns

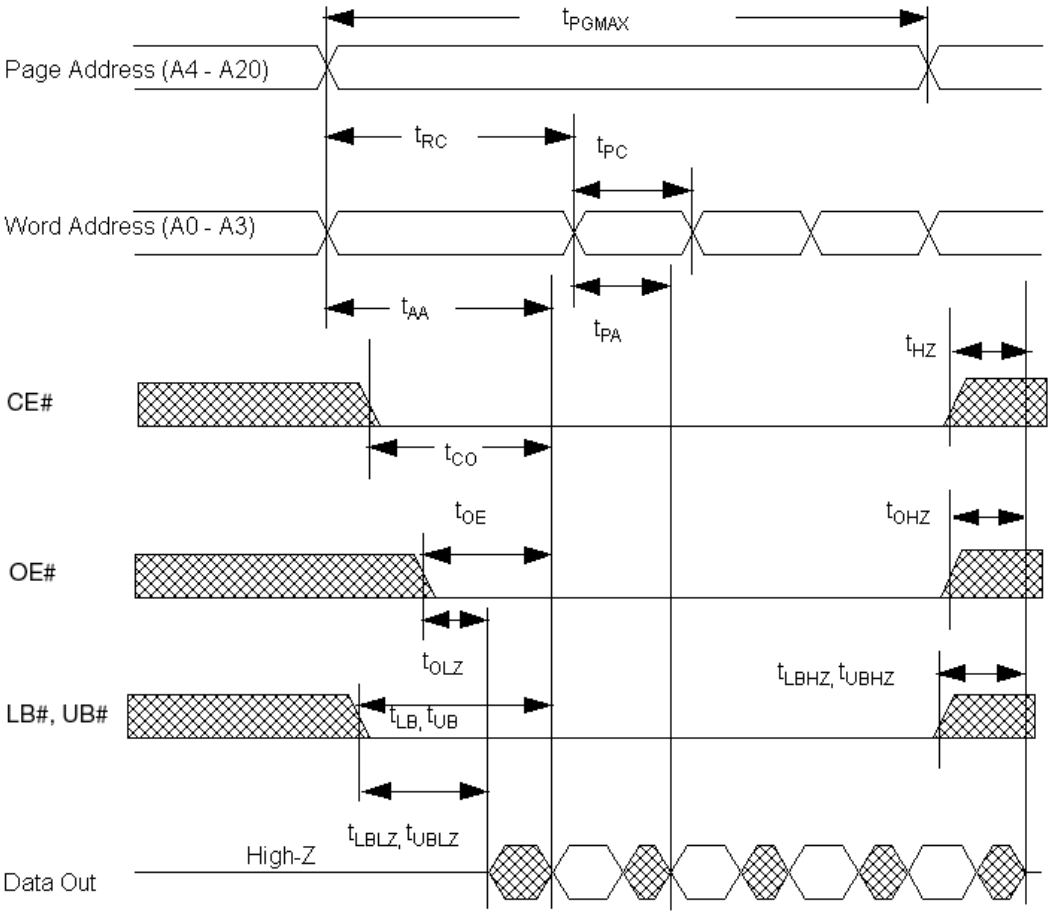
TIMING OF READ CYCLE (CE# = OE# = V_{IL}, WE# = V_{IH})



TIMING WAVEFORM OF READ CYCLE (WE#=V_{IH})

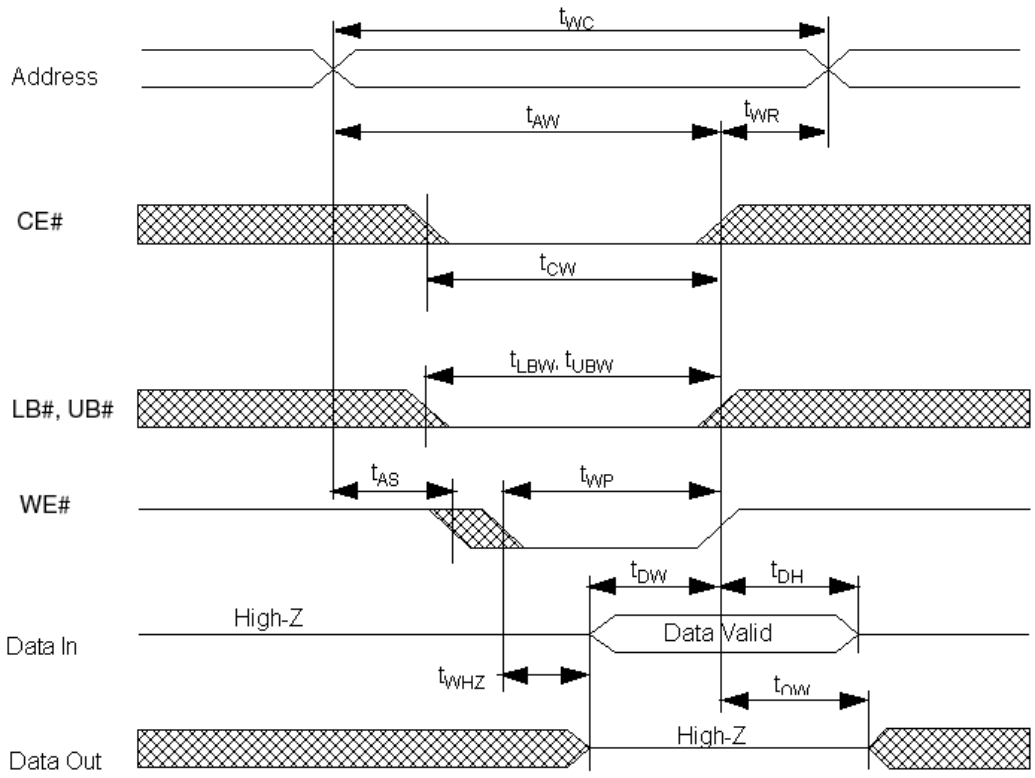


TIMING WAVEFORM OF PAGE MODE READ CYCLE (WE# = V_{IH})

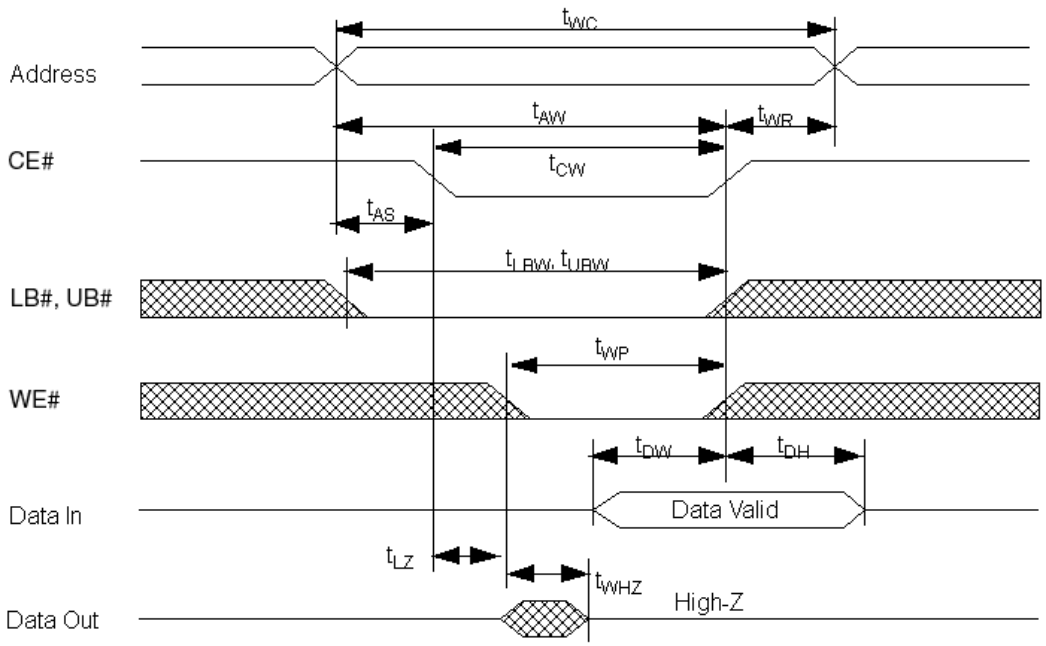


t_{PGMAX} means any page address (A4-A20) must be changed at least once in a 20us period

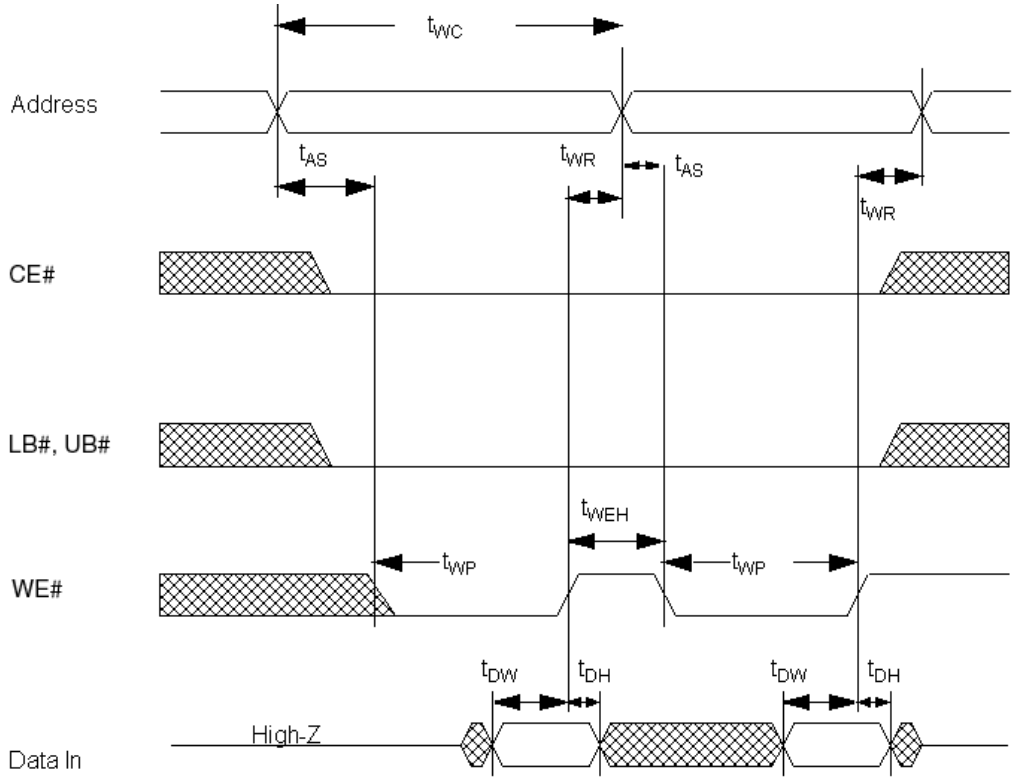
TIMING WAVEFORM OF WRITE CYCLE (WE# CONTROL)



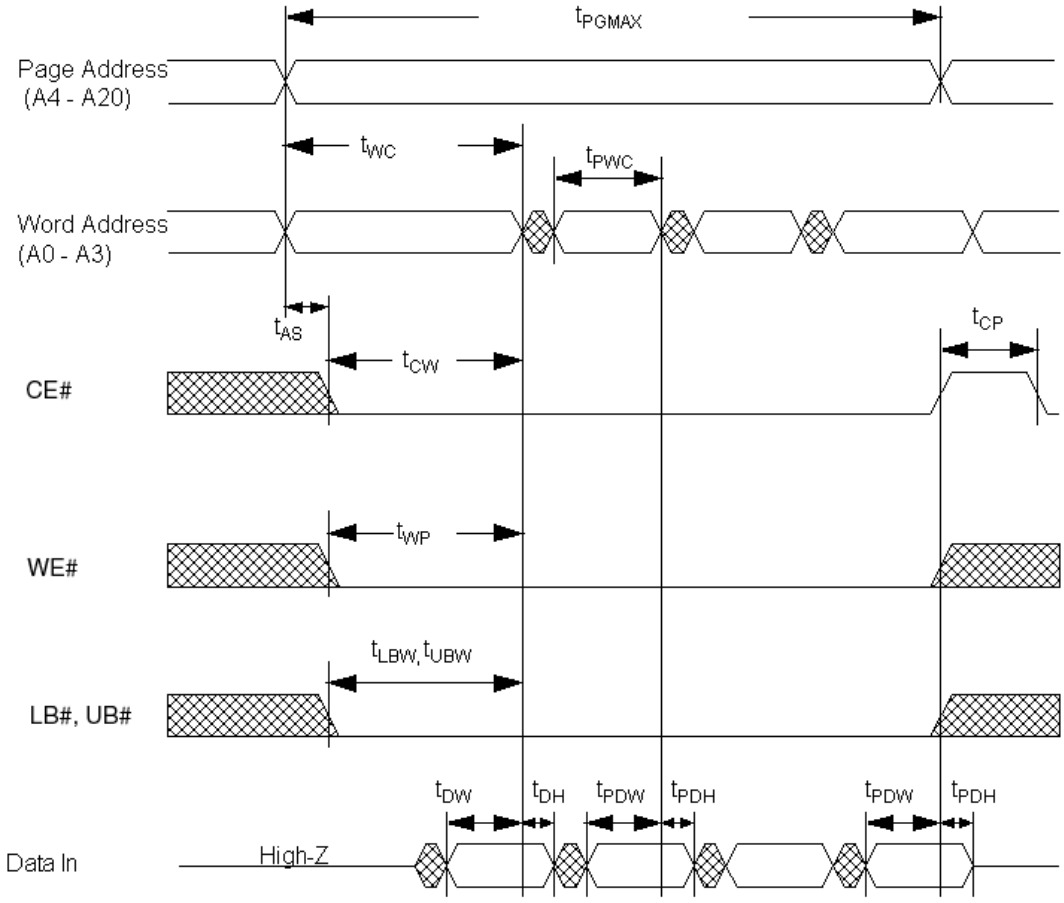
TIMING WAVEFORM OF WRITE CYCLE (CE# CONTROL)



TIMING WAVEFORM FOR SUCCESSIVE WE# WRITE CYCLES



TIMING WAVEFORM OF PAGE MODE WRITE CYCLE



t_{PGMAX} means any page address (A4-A20) must be changed at least once in a 20us period

POWER SAVINGS MODES

The PSRAM has three power savings modes:

- Reduced Memory Size
- Partial Array Refresh
- Deep Sleep Mode

The operation of the power saving modes is controlled by setting the Variable Address Register (VAR). This VAR is used to enable/disable the various low power modes.

The VAR is set by using the timings. The register must be set in less then 1µs after ZZ# is enabled low.

Reduced Memory Size (RMS)

In this mode of operation, the 32Mb PSRAM can be operated as a 8Mb, 16Mb or a 24Mb device. The mode and array size are determined by the settings in the VA register. The VA register is set according to the timings and the bit settings. The RMS mode is enabled at the time of ZZ# transitioning high and the mode remains active until the register is updated. To return to the full 32Mb address space, the VA register must be reset using the previously defined procedures.

Partial Array Refresh (PAR)

In this mode, the internal refresh operation can be restricted to a 8Mb, 16Mb or 24Mb portion of the array. The mode and array partition to be refreshed are determined by the settings in the VAR register. The VAR register is set according to the timings and the bit settings. In this mode, when ZZ# is taken low, only the portion of the array that is set in the register is refreshed. The operating mode is only available during standby time and once ZZ# is returned high, the device resumes full array refresh. All future PAR cycles will use the contents of the VA register. To change the address space of the PAR mode, the VA register must be reset using the previously defined procedures.

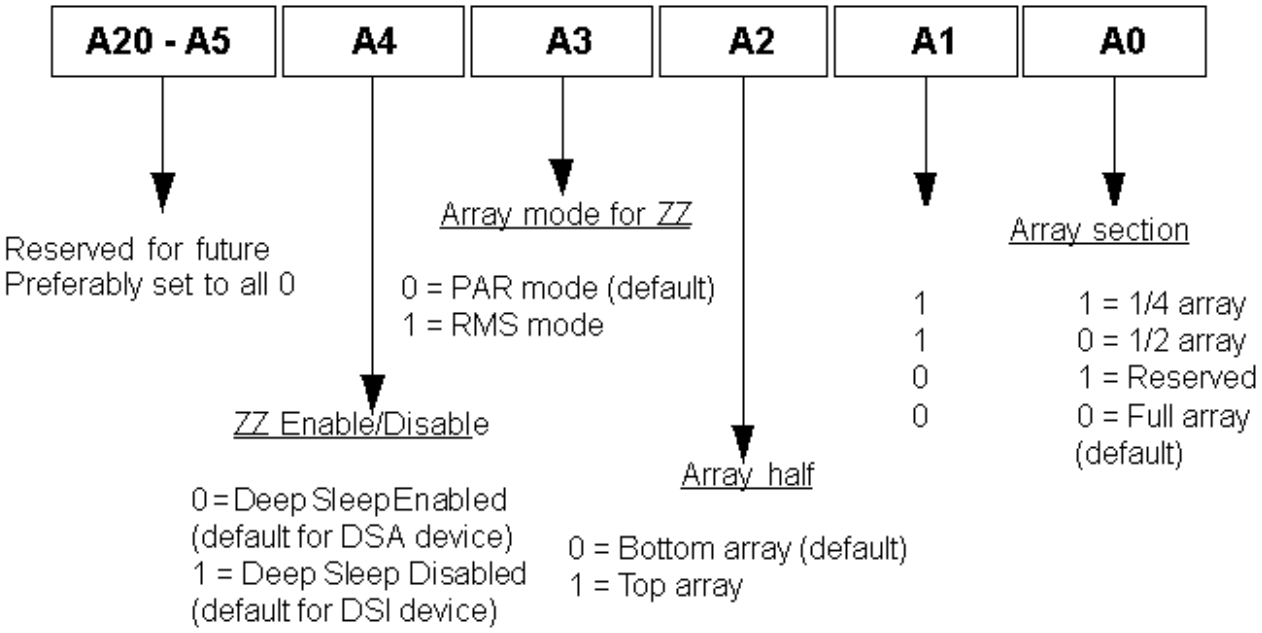
The default state for the ZZ# register will be such that ZZ# low will put the device into PAR mode after 1µs and never initiate a deep sleep mode unless appropri-

ate register is updated. This device is referred to as Deep Sleep Inactive, or DSI device. In either device, once the SRAM enters Deep Sleep Mode, the VAR contents are destroyed and the default register settings are reset.

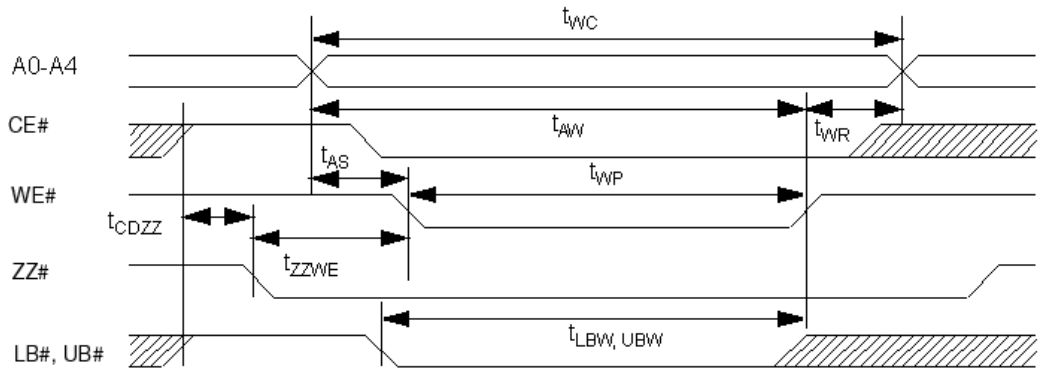
Deep Sleep Mode

In this mode of operation, the internal refresh is turned off and all data integrity of the array is lost. Deep Sleep is entered by bringing ZZ# low. After 1 µs, if the VAR register corresponding to A4 is not set to Deep Sleep Disabled, the device will enter Deep Sleep Mode. The device will remain in this mode as long as ZZ# remains low.

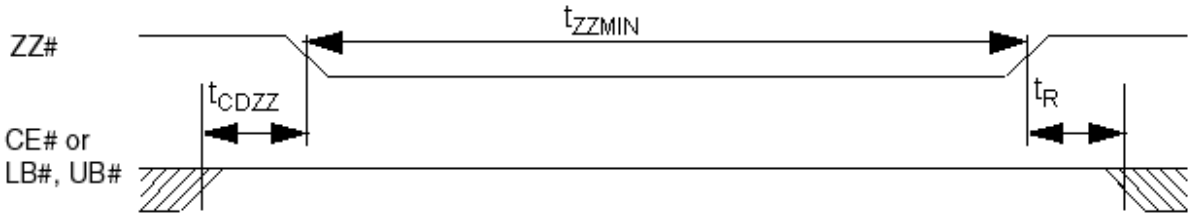
VARIABLE ADDRESS REGISTER



VARIABLE ADDRESS REGISTER (VAR) UPDATE TIMINGS



DEEP SLEEP MODE - ENTRY/EXIT TIMINGS



VAR UPDATE AND DEEP SLEEP TIMINGS

Item	Symbol	Min	Max	Unit
PAR and RMS ZZ# low to WE# low	t_{zzwe}		1000	ns
Chip (CE#, UB#/LB#) deselect to ZZ# low	t_{cdzz}	0		ns
Deep Sleep Mode	t_{zzmin}	10		ns
Deep Sleep Recovery	t_r	200		ns

ADDRESS PATTERNS FOR PAR (A3 = 0, A4 = 1)

A2	A1	A0	Active Section	Address Space	Size	Density
0	1	1	One-quarter of die	000000h - 07FFFFh	512Kb x 16	8Mb
0	1	0	One-half of die	000000h - 0FFFFFh	1Mb x 16	16Mb
x	0	0	Full Die	000000h-1FFFFFh	2Mbx16	32Mb
1	1	1	One-quarter of die	180000h - 1FFFFFh	512Kb x 16	8Mb
1	1	0	One-half of die	100000h - 1FFFFFh	1Mb x 16	16Mb

ADDRESS PATTERNS FOR RMS (A3 = 1, A4 = 1)

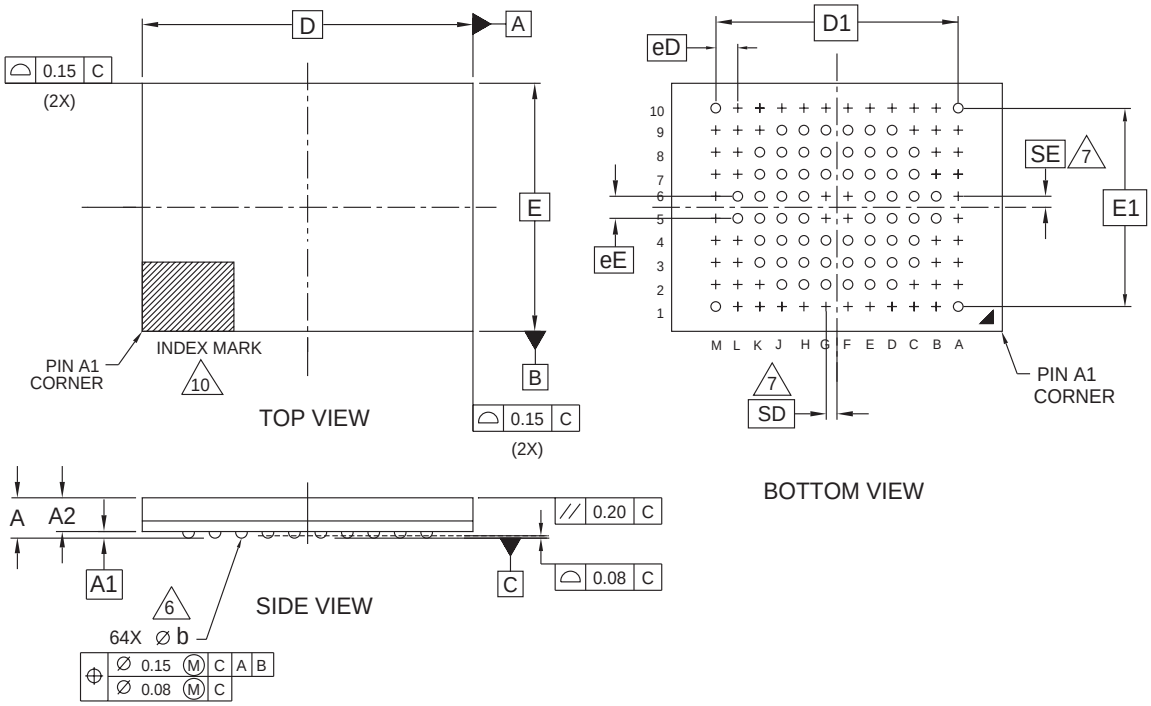
A2	A1	A0	Active Section	Address Space	Size	Density
0	1	1	One-quarter of die	000000h - 07FFFFh	512Kb x 16	8Mb
0	1	0	One-half of die	000000h - 0FFFFFh	1Mb x 16	16Mb
X	0	0	Full die	000000h - 1FFFFFh	2Mb x 16	32Mb
1	1	1	One-quarter of die	180000h - 1FFFFFh	512Kb x 16	8Mb
1	1	0	One-half of die	100000h - 1FFFFFh	1Mb x 16	16Mb

LOW POWER ICC CHARACTERISTICS FOR PSRAM

Item	Symbol	Test	Array Partition	Typ	Max	Unit
PAR Mode Standby Current	I_{PAR}	V_{IN} = V_{CC} or 0V, Chip Disabled, t_A= 85°C	1/4 Array	50	75	µA
			1/2 Array	70	90	
RMS Mode Standby Current	I_{RMSSB}	V_{IN} = V_{CC} or 0V, Chip Disabled, t_A= 85°C	8Mb Device	50	75	µA
			16Mb Device	70	90	
Deep Sleep Current	I_{ZZ}	VIN = VCC or 0V, Chip in ZZ# mode, t_A= 85°C		7	10	µA

PHYSICAL DIMENSIONS

TLD064–64-Ball Fine-pitch Ball Grid Array



PACKAGE	TLD 064			
JEDEC	N/A			
D x E	12.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.10	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		12.00 BSC.		BODY SIZE
E		9.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		64		BALL COUNT
ϕb	0.35	---	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B2,B3,B4,B7,B8,B9,B10 C1,C2,C9,C10,D1,D10,E1,E10 F1,F5,F6,F10,G1,G5,G6,G10 H1,H10,J1,J10,K1,K2,K9,K10 L1,L2,L3,L4,L7,L8,L9,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3309 \ 16-038.22a

REVISION SUMMARY

Revision A (January 22, 2004)

Initial release.

Revision A+1 (January 29, 2004)

Connection Diagrams

Corrected signal designation on ball H8.

AC Characteristics (Flash)

Read-only Operations: Added Figure 14.

pSRAM AC Characteristics

Figure 32, Write Timing #1 (Basic Timing): Renamed t_{WRC} to t_{AH}; extended t_{WR} to where WE# returns low; extended t_{BR} to where LB#, UB# goes low.

Figure 33, Write Timing #2 (WE# Control): The period along WE# formerly labeled t_{WR} is now t_{AH}. A new t_{WR} period has been added which extends from WE# going high after the first t_{WP} period to where the second t_{WP} period begins.

Figure 34, Write Timing #3-1 (WE#/LB#/UB# Byte Write Control): t_{WR} has been extended to where WE# returns low.

Figure 35, Write Timing #3-2 (WE#/LB#/UB# Byte Write Control): t_{WR} has been extended to where WE# returns low.

Write Operations table: Changed minimum specification for t_{WR} from 12 to 7.5 ns. Added t_{AH} specification.

Revision A+2 (February 16, 2004)

PSRAM Features

Feature list was corrected to four main features

Lookahead Pinout Diagram

Figure was removed and replaced by TBD.

Ordering Information

Added and option that designates standard or second supplier for PSRAM.

AM49LV128BM MCP with Second Supplier

Section added.

Revision A+3 (February 25, 2004)

Operating Ranges

Removed V_{IO} from the list of supply voltages.

AM49LVxxxBM MCP with Second Supplier PSRAM Block Diagram

Added a note clarifying ZZ#.

Revision A+4 (March 4, 2004)

Lookahead Diagram

Added the lookahead diagram.

Revision A+5 (March 15, 2004)

Global

Changed DQ designations to 0-7 and 8-15.

Global

Removed references to the 4M Partial power down mode and added references to Deep Sleep.

Recommended Operating Conditions

Corrected Min. and Max values for V_{IH} parameter.

PSRAM AC Characteristics
Write Operation

Changed column head to Value, added t_{WHOL} parameter, changed min value of t_{BWO} to 30, and added Notes 8, 9, and 10.

AC Characteristics

Added Power Down Parameters and Other Timing Parameters tables.

AM49LV128BM MCP with Second PSRAM Supplier

Removed Capacitance section.

Partial Array Refresh (PAR)

Removed reference to two versions.

Revision A6 (June 17, 2004)

"Absolute Maximum Ratings" on page 37

Changed "Voltage on VCC Supply relative to VSS - Rating" To -0.2 to 3.6.

Changed "Power Dissipation - Rating" to 1.

Changed "Operating Temperature - Rating" to -25 to +85.

"Low Power ICC Characteristics for PSRAM" on page 93

Changed "PAR Mode Standby Current" - Type to "50" and Max to "75".

Changed "RMS Mode Standby Current - 8Mb Device" - Type to "50" and Max to "75".

Changed "RMS Mode Standby Current - 16Mb Device" - Type to "70" and Max to "90".

Changed "Deep Sleep Current" -Type to "7".

"Address Patterns for RMS (A3 = 1, A4 = 1)" on page 92

Deleted "Three-quarters of die from table.

Deleted “Full Die” from table.

“Address Patterns for PAR (A3 = 0, A4 = 1)” on page 91

Added “Full Die” to table.

“Timing” on page 79

Changed “Chip Disable to High-Z Output - Max” to 5.

Changed “Output Disable to High-Z Output - Max” to 5.

Changed “Byte Select Disable to High-Z Output - Max” to 5.

Changed “Write to High-Z Output - Max” to 5.

“Operating Characteristics (Over Specified Temperature Range)” on page 77

Changed “Supply Voltage for I/O - Min” to 7.7.

Changed “Input High Voltage - Min” to 0.8.

Changed “Output High Voltage - Max” to 0.2.

Changed “Output Low Voltage - Test Condition” to...=0.5mA.hanged “Output Low Voltage - Max.” to 0.2VccQ.

Changed “Input Leakage Current - Min.” to -1.

Changed “Input Leakage Current - Max.” to 1.

Changed “Output Leakage Current - Min.” to -1

Changed “Output Leakage Current - Max.” to 1.

Changed “Read/Write Operating Supply Current @1...-Test Condition” to Vcc=3.1V...

Changed “Read/Write Operating Supply Current @65...-Test Condition” to Vcc=3.1V...

Changed “Page Mode Operating Supply Current. - Test Condition” to Vcc=3.1V...

Changed “Page Mode Operating Supply Current. - Max.” to 25.0

Changed “Maximum Standby Current - Test Condition” to Vcc=3.1V...

Changed “Maximum Standby Current - Max.” to 120.

Colophon

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