



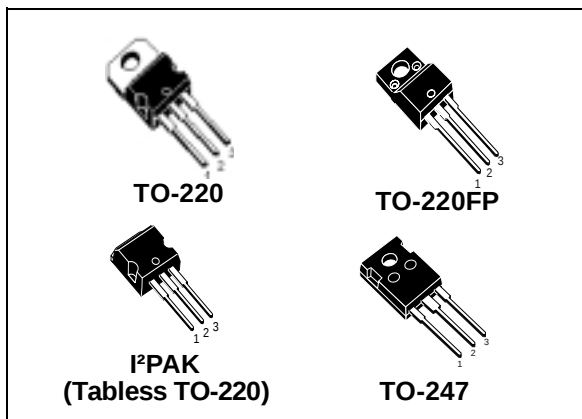
STP22NM50 - STF22NM50 STB22NM50-1 - STW22NM50

N-CHANNEL 550V@T_{jmax} - 0.16Ω - 20A TO-220/FP/I²PAK/TO-247
MDmesh™ MOSFET

ADVANCED DATA

TYPE	V _{DSS} (@T _{jmax})	R _{DS(on)}	R _{ds(on)} *Q _g	I _D
STP22NM50	550 V	<0.215Ω	6.4 Ω*nC	20 A
STF22NM50	550 V	<0.215Ω	6.4 Ω*nC	20 A
STB22NM50-1	550 V	<0.215Ω	6.4 Ω*nC	20 A
STW22NM50	550 V	<0.215Ω	6.4 Ω*nC	20 A

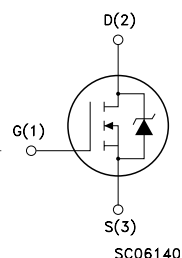
- TYPICAL R_{DS(on)} = 0.16Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE



DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP22NM50	P22NM50	TO-220	TUBE
STF22NM50	F22NM50	TO-220FP	TUBE
STB22NM50-1	B22NM50-1	I ² PAK	TUBE
STW22NM50	W22NM50	TO-247	TUBE

STP22NM50 - STF22NM50 - STB22NM50-1 - STW22NM50

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		STP22NM50 STB22NM50-1	STF22NM50	STW22NM50	
V_{GS}	Gate-source Voltage	± 30			V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	20	20(*)	20	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	12.6	12.6(*)	12.6	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	80	80(*)	80	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	192	45	210	W
	Derating Factor	1.2	0.36	1.2	W/ $^\circ\text{C}$
dv/dt (1)	Peak Diode Recovery voltage slope	15			V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	--	2000		V
T_{stg}	Storage Temperature	-65 to 150			$^\circ\text{C}$
T_j	Max. Operating Junction Temperature	150			$^\circ\text{C}$

($\bullet$) Pulse width limited by safe operating area.

(1) $I_{SD} \leq 20\text{A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

(*) Limited only by maximum temperature allowed.

THERMAL DATA

		TO-220/1 ² PAK/TO-247	TO-220FP	
$R_{thj-case}$	Thermal Resistance Junction-case Max	0.65	2.8	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	62.5		$^\circ\text{C}/\text{W}$
T_l	Maximum Lead Temperature For Soldering Purpose	300		$^\circ\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	10	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = 5\text{ A}$, $V_{DD} = 50\text{ V}$)	650	mJ

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.16	0.215	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 10A$		10		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1\text{ MHz}$, $V_{GS} = 0$		1480 285 34		pF pF pF
$C_{oss\text{ eq.}}$ (2)	Equivalent Output Capacitance	$V_{GS} = 0V$, $V_{DS} = 0V$ to $400V$		130		pF
R_g	Gate Input Resistance	$f=1\text{ MHz}$ Gate DC Bias=0 Test Signal Level=20mV Open Drain		1.6		Ω

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250\text{ V}$, $I_D = 10\text{ A}$		24		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		16		ns
Q_g	Total Gate Charge	$V_{DD} = 400\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$		40	56	nC
Q_{gs}	Gate-Source Charge			13		nC
Q_{gd}	Gate-Drain Charge			19		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400\text{ V}$, $I_D = 20\text{ A}$,		9		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 5)		8.5		ns
t_c	Cross-over Time			23		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				20	A
I_{SDM} (2)	Source-drain Current (pulsed)				80	A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 20\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 20\text{ A}$, $di/dt = 100A/\mu s$,		350		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 100\text{ V}$, $T_j = 25^\circ C$		4.6		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		26		A
t_{rr}	Reverse Recovery Time	$I_{SD} = 20\text{ A}$, $di/dt = 100A/\mu s$,		435		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 100\text{ V}$, $T_j = 150^\circ C$		5.9		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		27		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

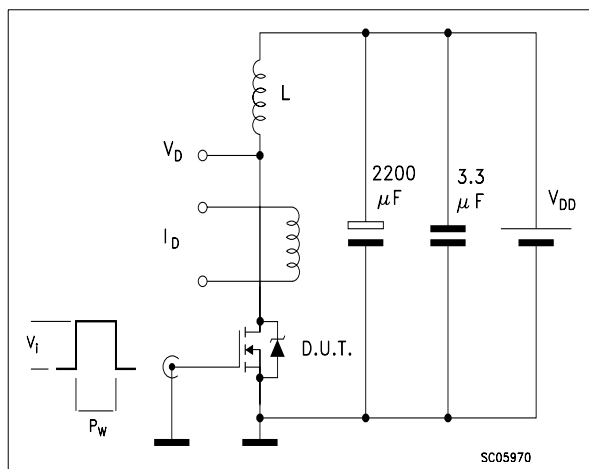


Fig. 2: Unclamped Inductive Waveform

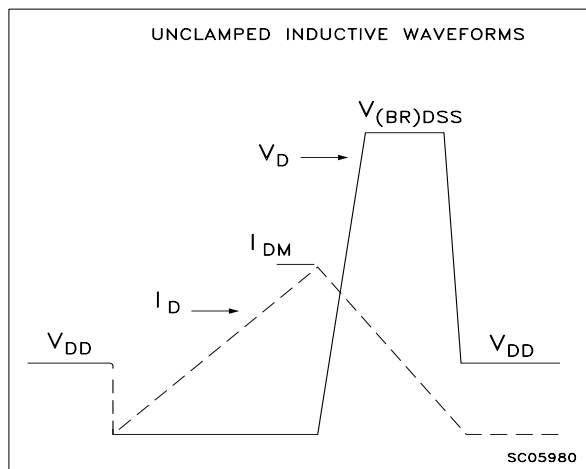


Fig. 3: Switching Times Test Circuit For Resistive Load

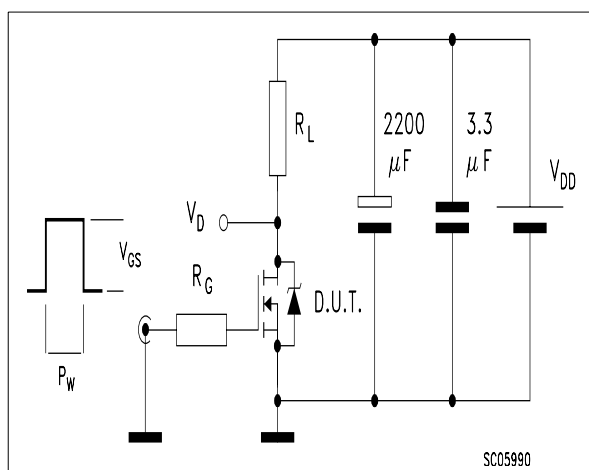


Fig. 4: Gate Charge test Circuit

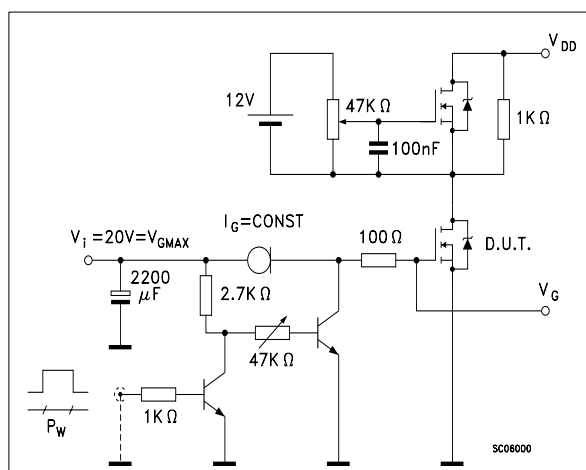
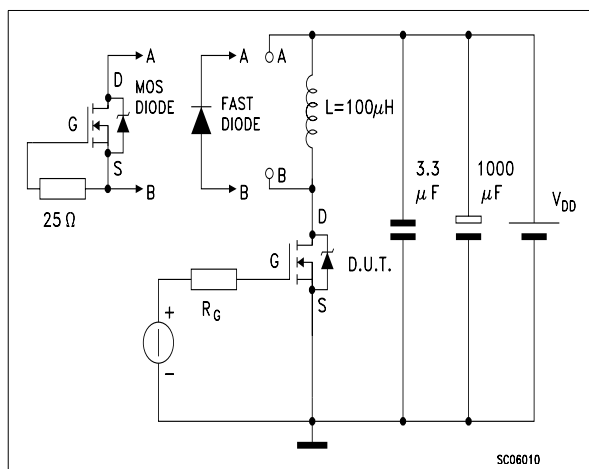
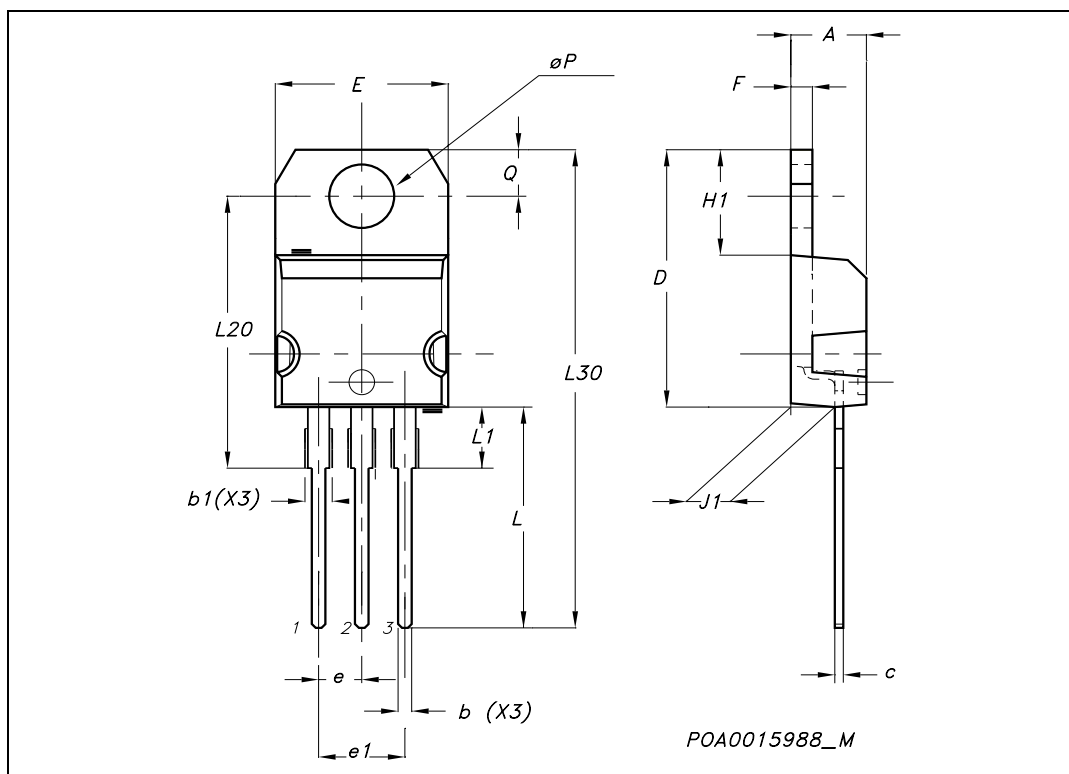


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



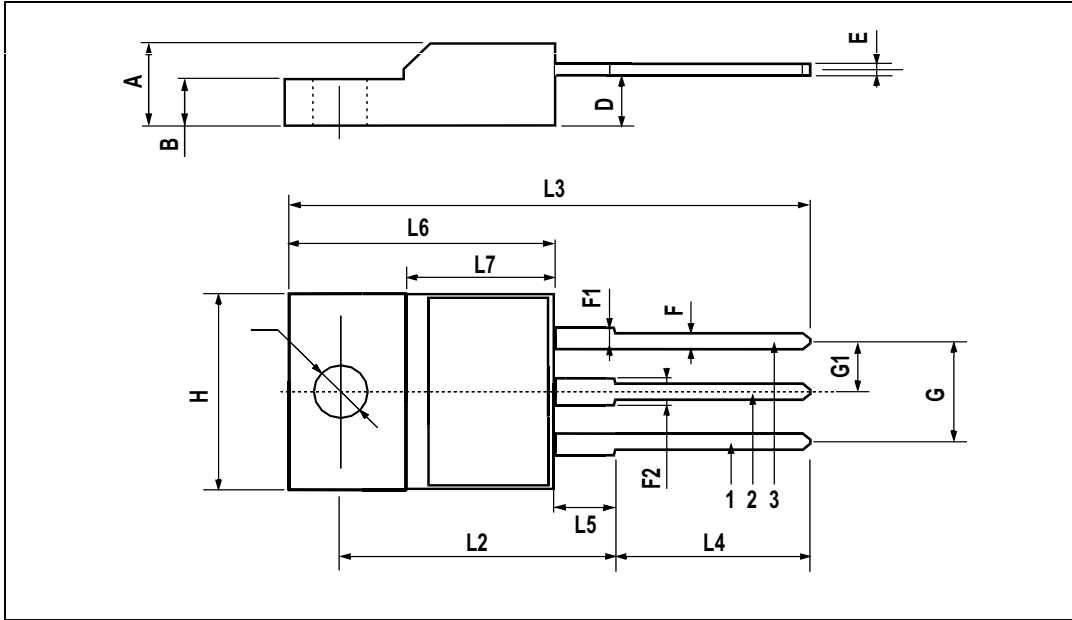
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



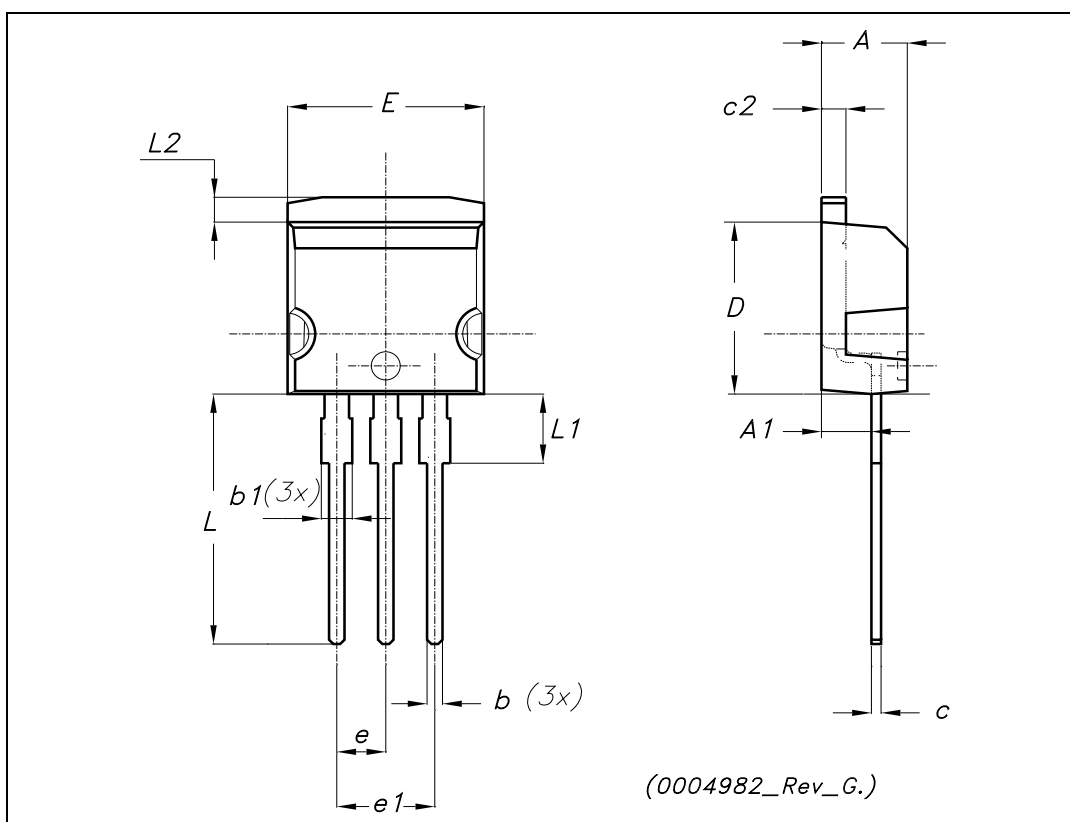
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



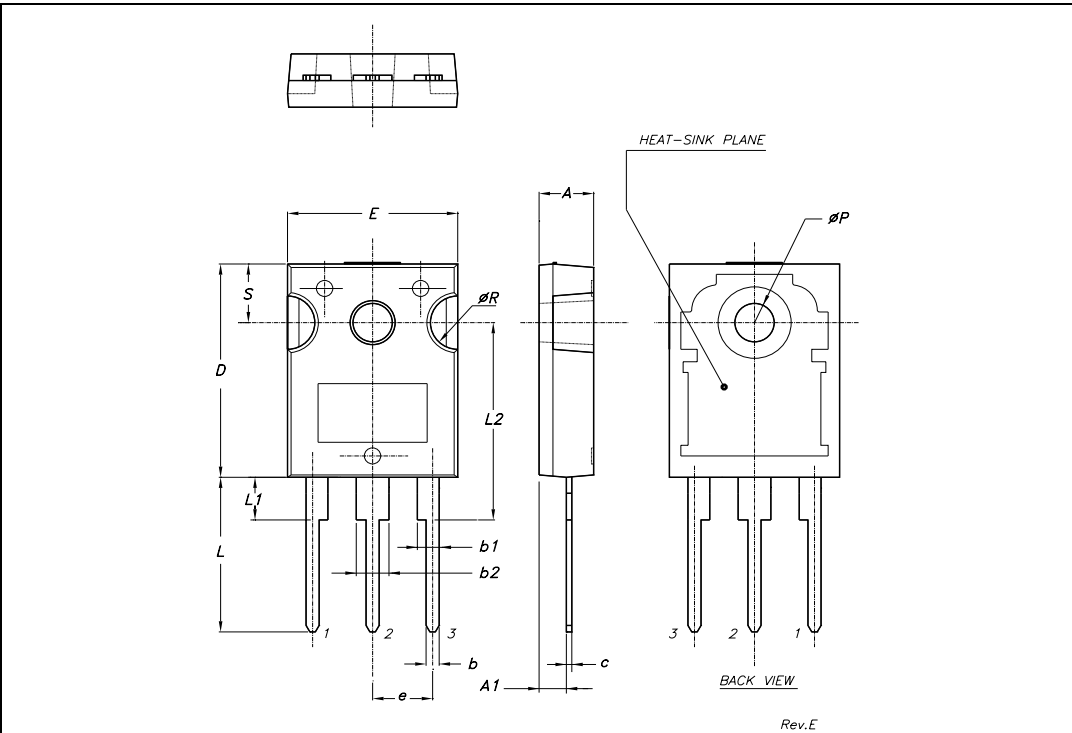
TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



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