

LH5P860

CMOS 512K (64K × 8) Pseudo-Static RAM

FEATURES

- 65,536 × 8 bit organization
- Access time: 80 ns (MAX.)
- Cycle time: 140 ns (MIN.)
- Single +5 V power supply
- Pin compatible with 1M standard SRAM
- Power consumption (MAX.):
 - Operating: 440 mW
 - Self refresh (TTL level): 5.5 mW
 - Self refresh (CMOS level): 2.75 mW
- TTL compatible I/O
- 512 refresh cycles/8 ms (MAX.)
- Available for auto-refresh and self-refresh modes
- Packages:
 - 32-pin, 600-mil DIP
 - 32-pin, 525-mil SOP

DESCRIPTION

The LH5P860 is a 512K-bit Pseudo-Static RAM organized as 65,536 × 8 bits. It is fabricated using silicon-gate CMOS process technology. With its built-in oscillator, it is easy to refresh memories without an external clock.

PIN CONNECTIONS

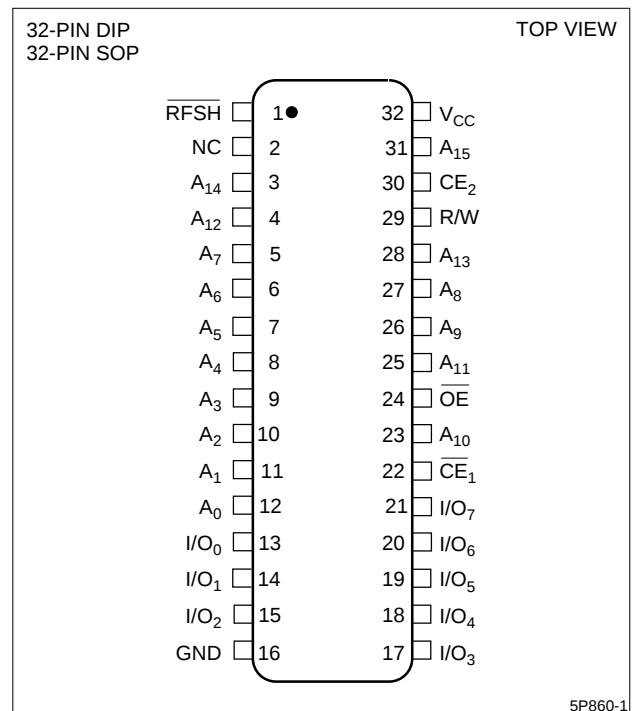


Figure 1. Pin Connections for DIP and SOP Packages

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on all pins	V_T	−1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power dissipation	P_D	600	mW	
Operating temperature	T_{opr}	0 to +70	°C	
Storage temperature	T_{stg}	−65 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		$V_{CC} + 0.3$	V
	V_{IL}	−1.0		0.8	V

CAPACITANCE ($T_A = 0$ to +70°C, $f = 1$ MHz, $V_{CC} = 5.0$ V $\pm 10\%$)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	$A_0 - A_{15}$	C_{IN1}		8	pF
	R/W, OE, RFSH	C_{IN2}		5	pF
	CE_1, CE_2	C_{IN3}		5	pF
Input/Output capacitance	$I/O_0 - I/O_7$	C_{OUT1}		10	pF

DC CHARACTERISTICS ($T_A = 0$ to +70°C, $V_{CC} = 5.0$ V $\pm 10\%$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	I_{CC1}			80	mA	1, 2
Supply current in standby mode	I_{CC2}	TTL input		1.0	mA	1, 3
		CMOS input		0.5		1, 4
Average supply current in self refresh cycle	I_{CC3}	TTL input		1.0	mA	1, 5
		CMOS input		0.5		1, 6
Input leakage current	I_{LI}	$0\text{ V} \leq V_{IN} \leq 6.5\text{ V}$, 0 V except on test pins	−10	10	μA	
I/O leakage current	I_{LO}	$0\text{ V} \leq V_{OUT} \leq V_{CC} + 0.3\text{ V}$, Outputs in high-impedance state	−10	10	μA	
Output HIGH voltage	V_{OH}	$I_{OUT} = -1.0\text{ mA}$	2.4		V	
Output LOW voltage	V_{OL}	$I_{OUT} = 4.0\text{ mA}$		0.4	V	

NOTES:

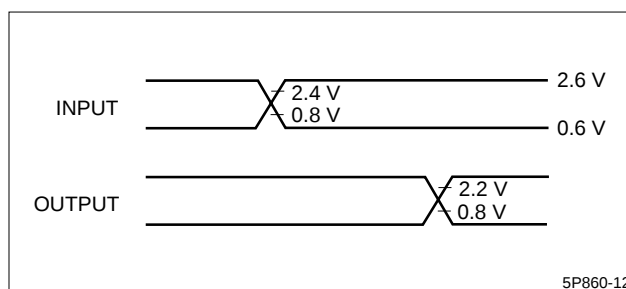
1. Specified values are with outputs open.
2. I_{CC1} depends on the cycle time.
3. $CE_1 = V_{IH}$, RFSH = V_{IH} .
4. $CE_1 = V_{CC} - 0.2\text{ V}$, RFSH = $V_{CC} - 0.2\text{ V}$.
5. $CE_1 = V_{IH}$, RFSH = V_{IL} .
6. $CE_1 = V_{CC} - 0.2\text{ V}$, RFSH = 0.2 V .

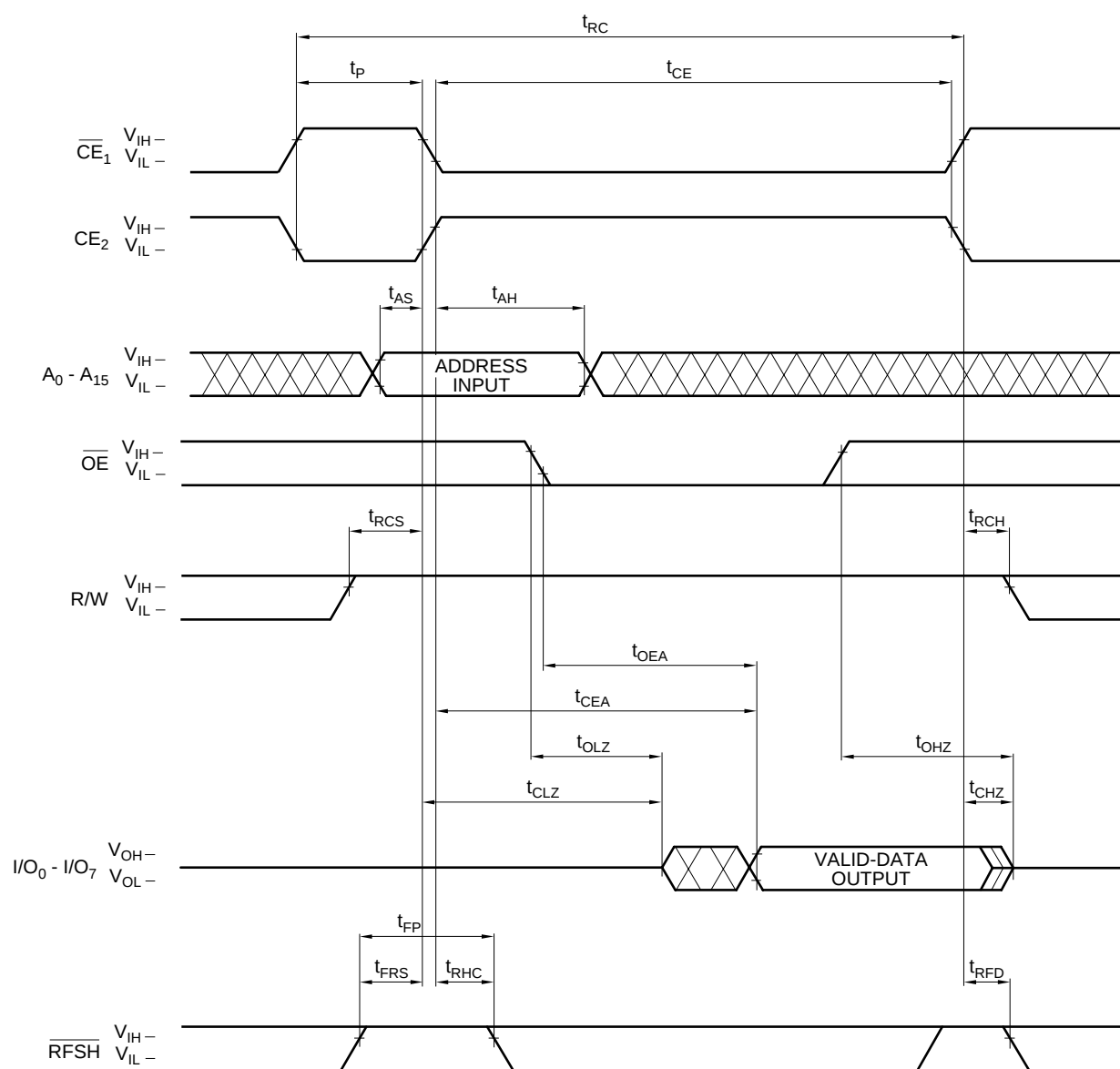
AC CHARACTERISTICS ^{1, 2, 3} ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Random read, write cycle time	t_{RC}	140		ns	
Read modify write cycle time	t_{RMW}	205		ns	
CE pulse width	t_{CE}	80	10,000	ns	
CE precharge time	t_P	50		ns	
Address setup time	t_{AS}	0		ns	4
Address hold time	t_{AH}	20		ns	4
Read command setup time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
CE access time	t_{CEA}		80	ns	5
OE access time	t_{OEA}		30	ns	5
Output enable time from CE	t_{CLZ}	20		ns	
Output enable time from $\overline{OE}$	t_{OLZ}	0		ns	
Output enable time from R/W	t_{WLZ}	0		ns	
Output disable time from CE	t_{CHZ}		25	ns	
Output disable time from $\overline{OE}$	t_{OHZ}		25	ns	
Output disable time from R/W	t_{WHZ}		25	ns	
OE setup time	t_{OES}	10		ns	
$\overline{OE}$ hold time	t_{OEH}	10		ns	
Write command pulse width	t_{WP}	30		ns	
Write command setup time	t_{WCS}	30		ns	
Write command hold time	t_{WCH}	50		ns	
Data setup time from R/W	t_{DSW}	30		ns	6
Data setup time from CE	t_{DSC}	30		ns	6
Data hold time from R/W	t_{DHW}	0		ns	6
Data hold time from CE	t_{DHC}	0		ns	6
Transition time (rise and fall)	t_T	3	35	ns	
Refresh time interval	t_{REF}		8	ms	
Refresh command hold time	t_{RHC}	15		ns	
Auto refresh cycle time	t_{FC}	130		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	50		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		ns	
CE delay time from refresh precharge (Self refresh)	t_{FRS}	160		ns	

NOTES:

1. In order to initialize the circuit, an initialize pause of 100 μs with $CE_1 = V_{IH}$, $RFSH = V_{IH}$ (or $CE_2 = V_{IL}$, $RFSH = V_{IH}$) is required after power-up, followed by at least 8 dummy cycles.
2. AC characteristics are measured at $t_T = 5\text{ ns}$.
3. AC characteristics are measured at the following condition (see figure at right):
4. Address is latched at the negative edge of $\overline{CE}_1$ or at the positive edge of CE_2 .
5. Measured with a load equivalent to 2TTL + 100 pF.
6. Data is latched at the positive edge of R/W, at the positive edge of CE_1 , or at the negative edge of CE_2 .

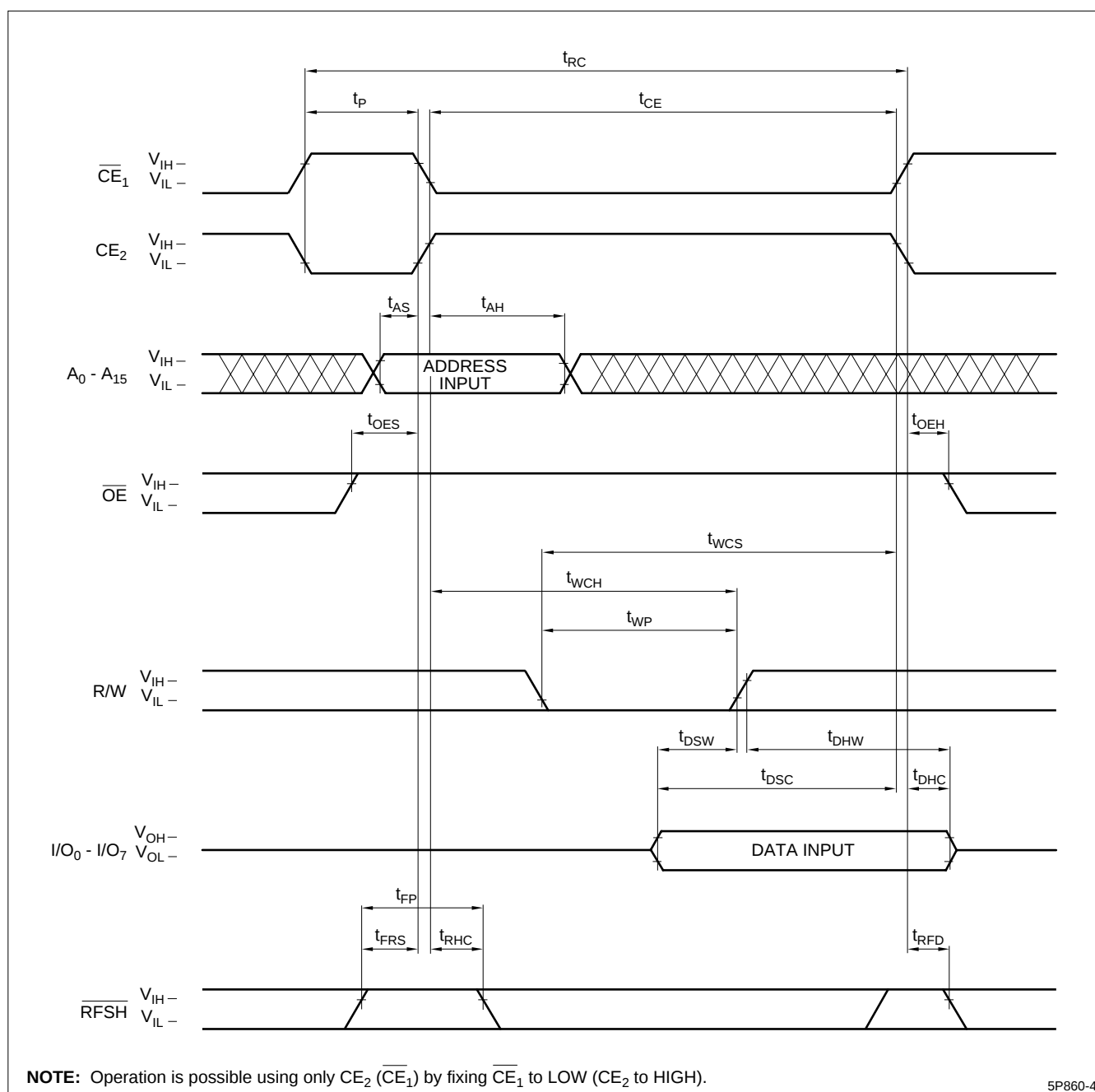
**Figure 3. AC Characteristics**



NOTE: Operation is possible using only CE_2 ($\overline{CE}_1$) by fixing $\overline{CE}_1$ to LOW (CE_2 to HIGH).

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Figure 4. Read Cycle

Figure 5. Write Cycle 1 ($\overline{OE}$ = Fix 'H')

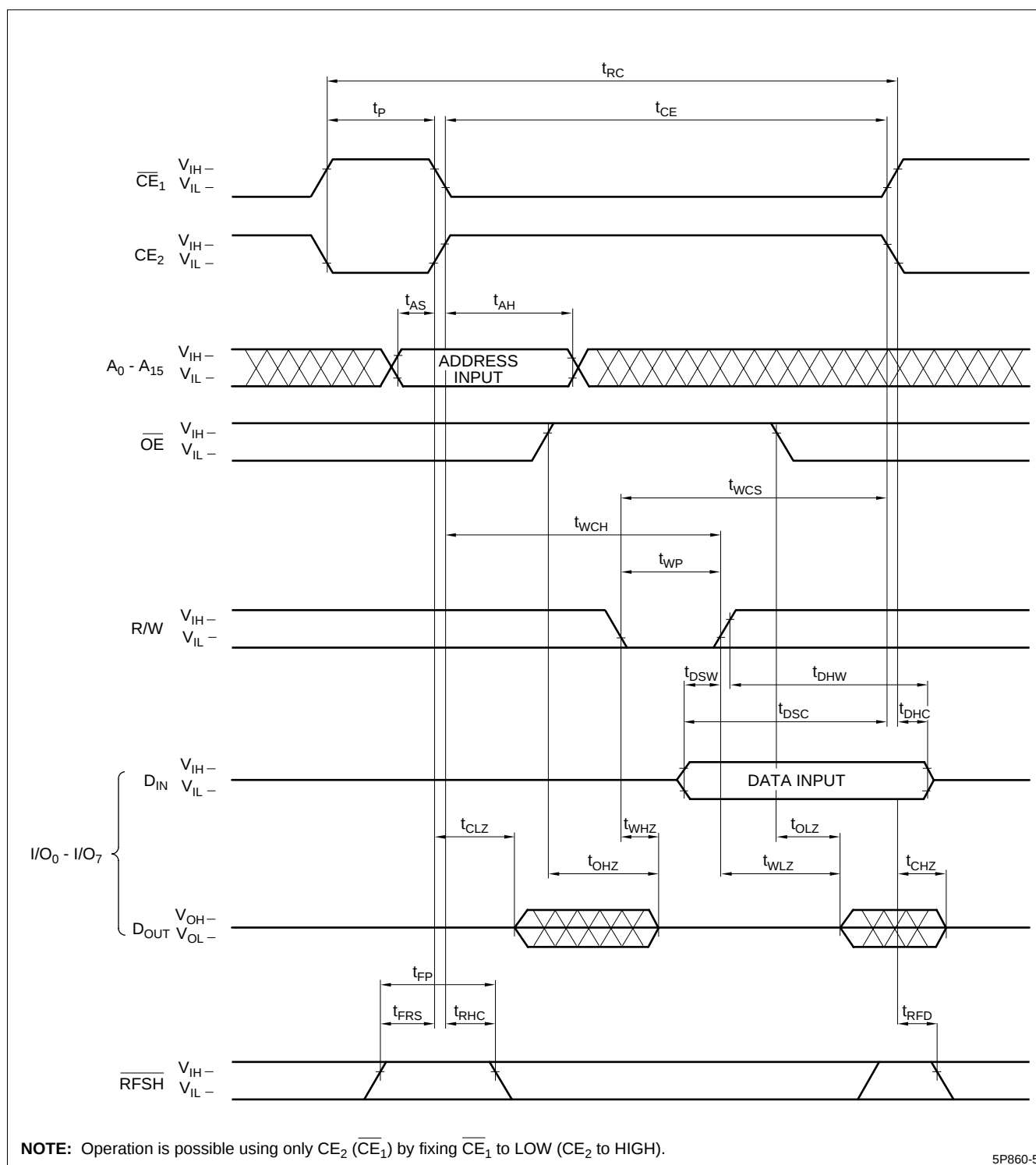
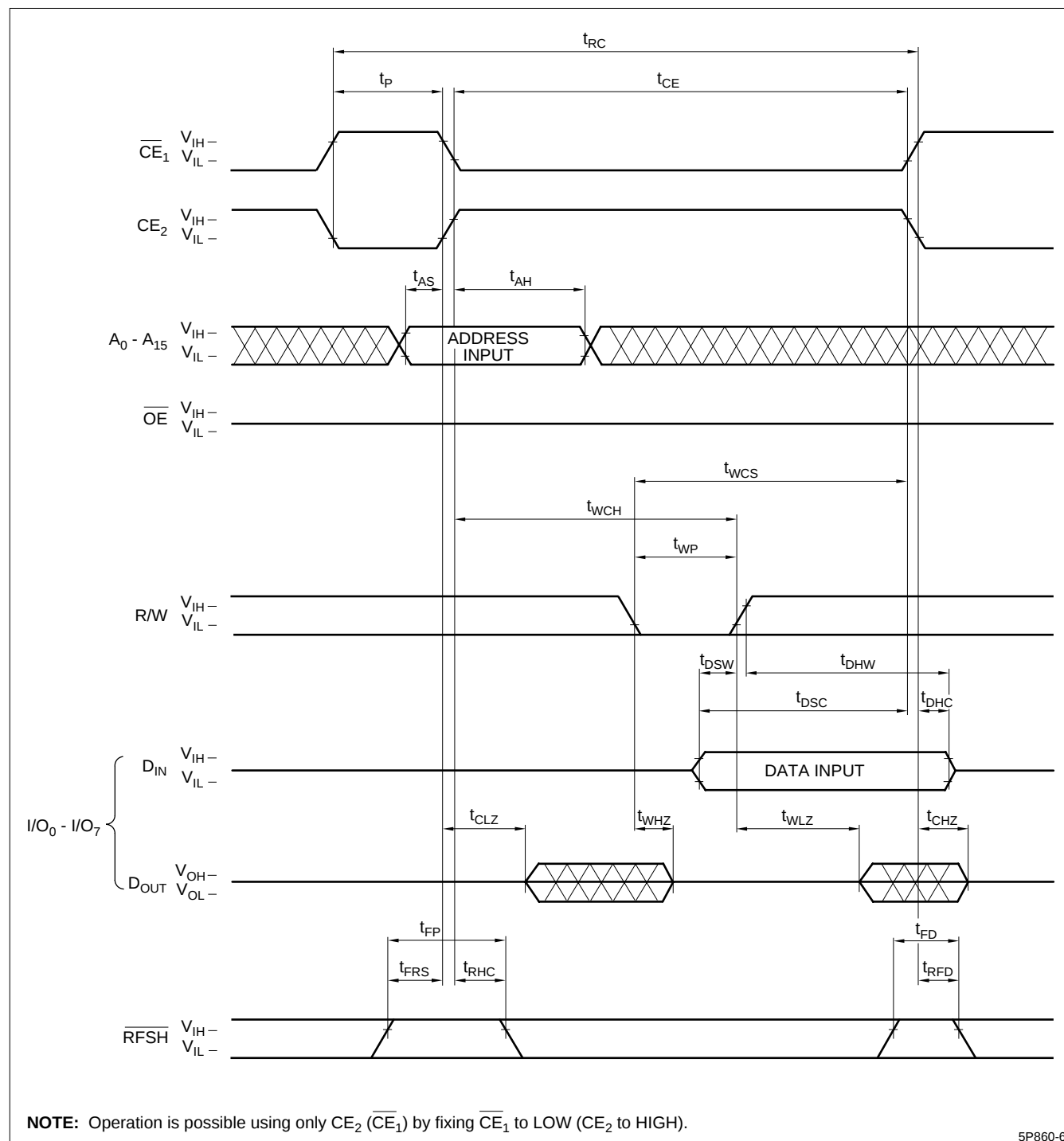


Figure 6. Write Cycle 2 (OE Clock)

Figure 7. Write Cycle 3 ($\overline{OE}$ = Fix 'L')

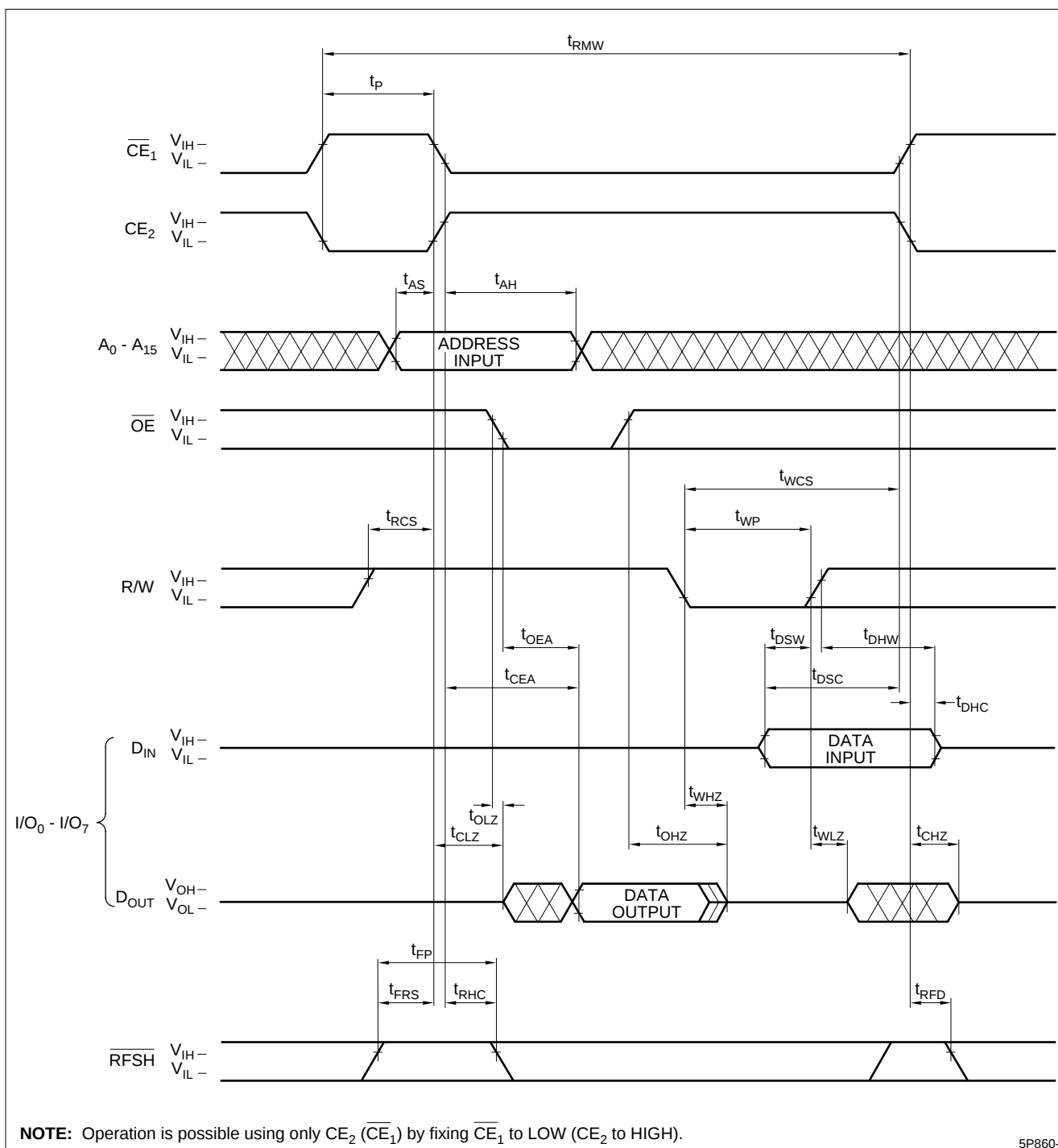
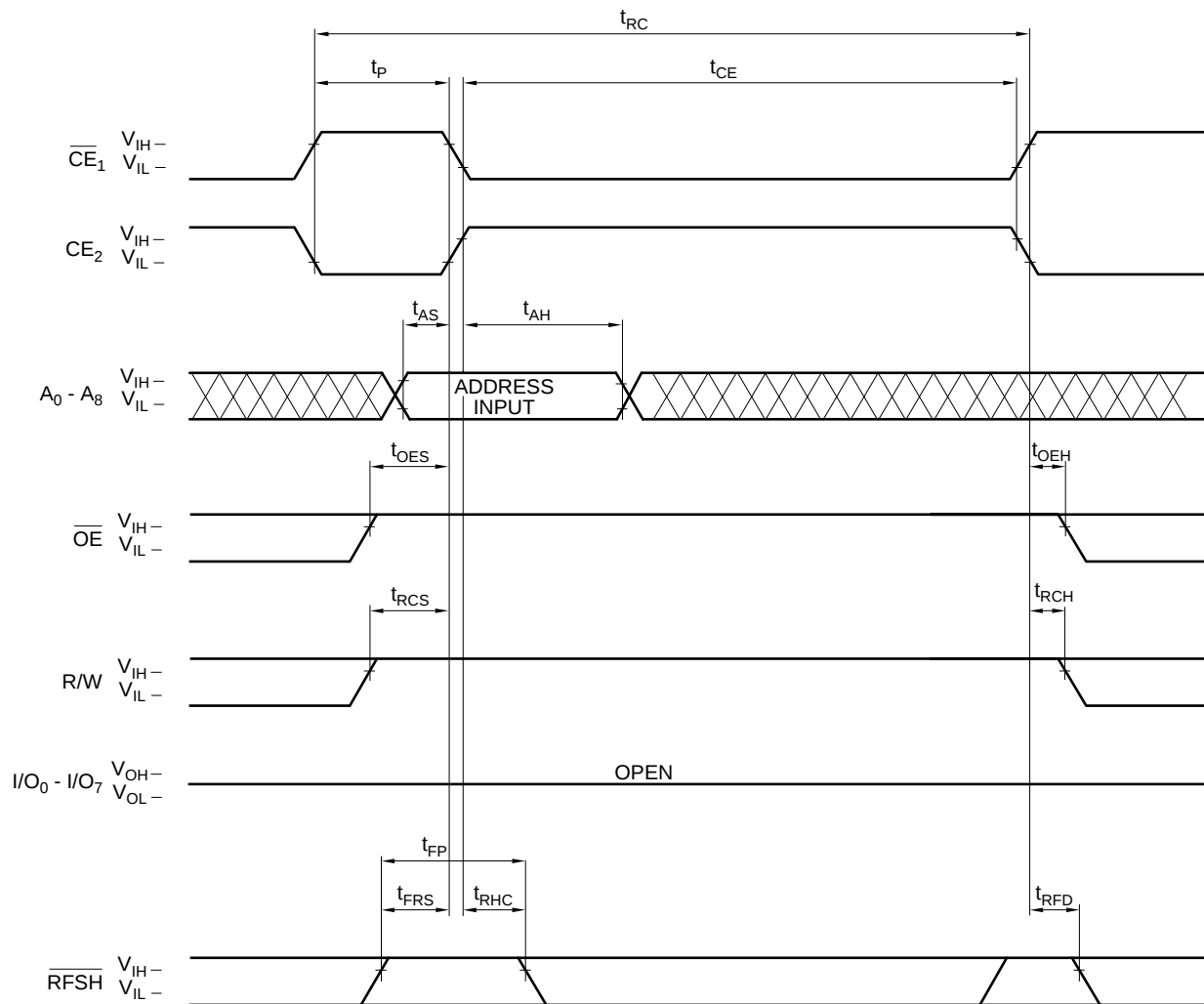


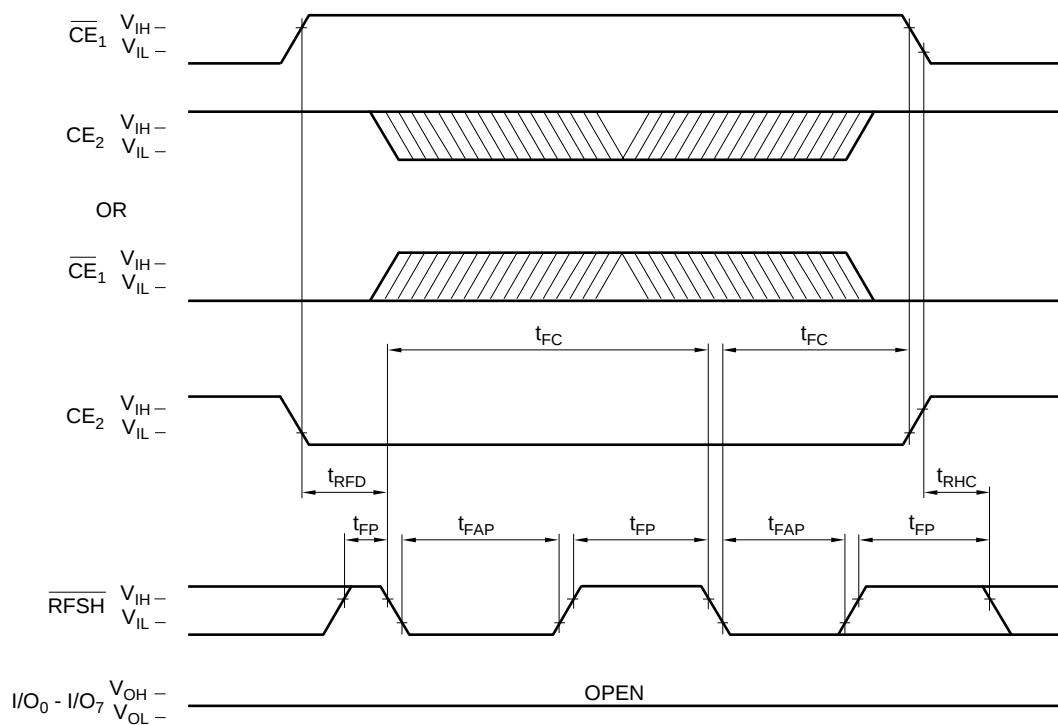
Figure 8. Read-Modify-Write Cycle

**NOTES:**

1. Operation is possible using only $\overline{CE}_2$ ($\overline{CE}_1$) by fixing $\overline{CE}_1$ to LOW ($\overline{CE}_2$ to HIGH).
2. $A_9 - A_{16}$ = Don't Care.

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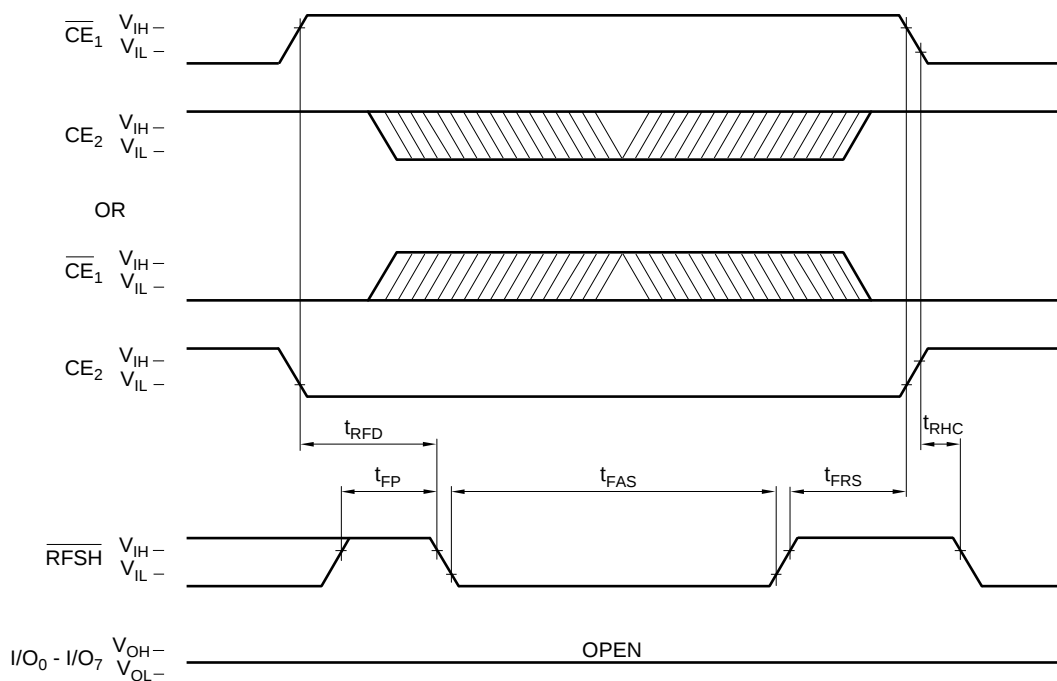
Figure 9. CE Only Refresh Cycle



NOTE: $\overline{OE}$, R/W , $A_0 - A_{16}$ = Don't care

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Figure 11. Auto Refresh Cycle

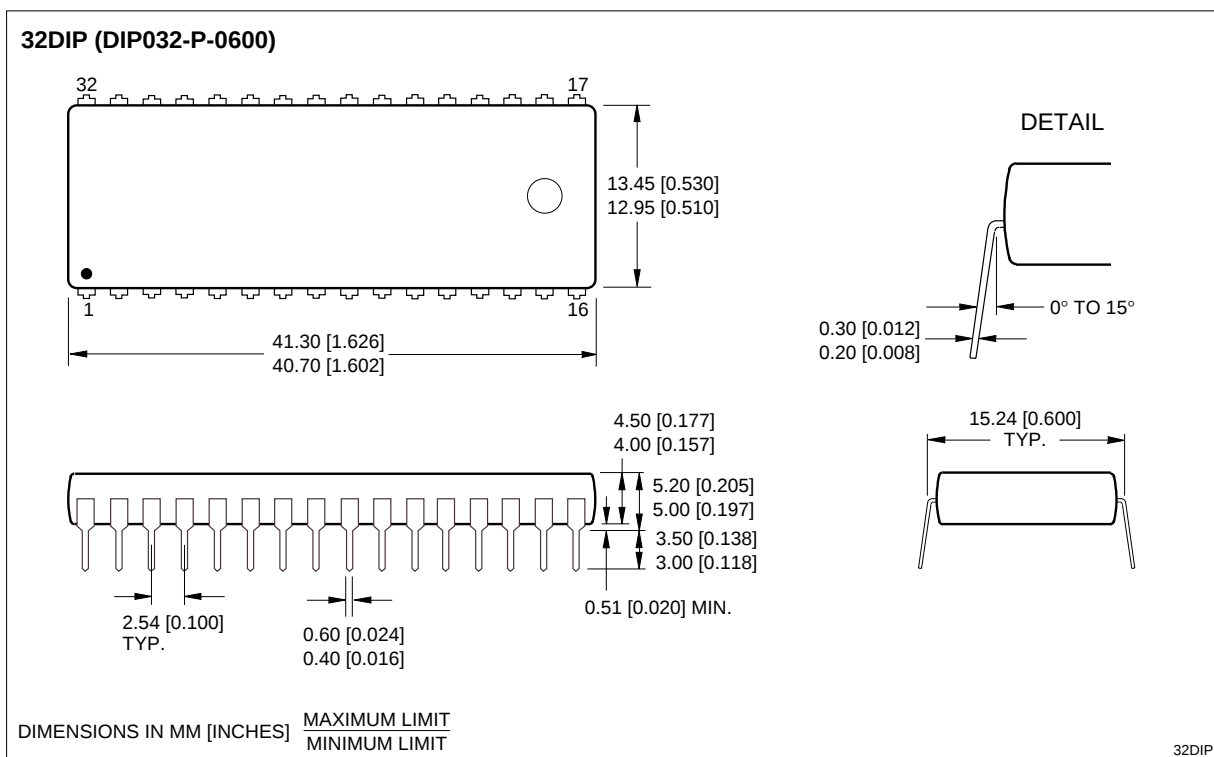


NOTE: $\overline{OE}$, R/W , $A_0 - A_{16}$ = Don't care

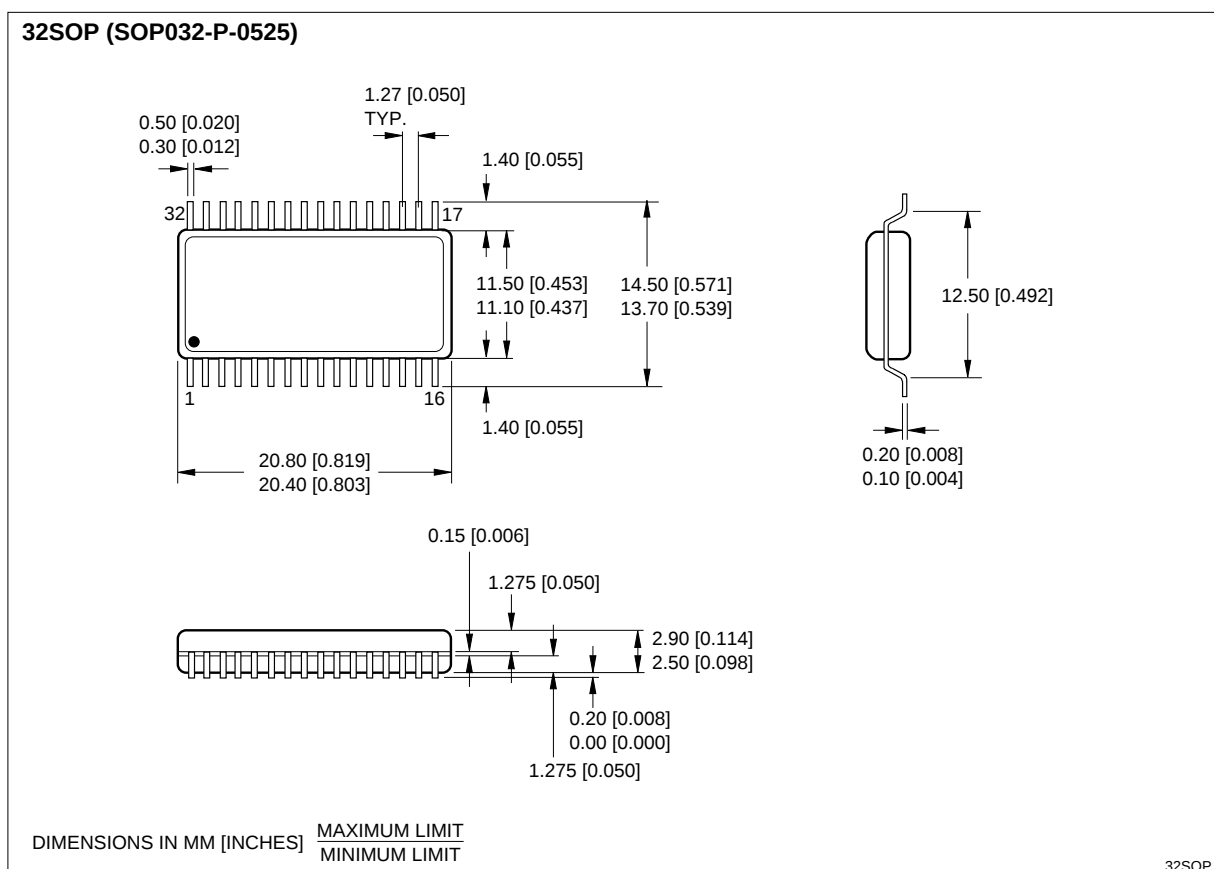
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Figure 10. Self Refresh Cycle

PACKAGE DIAGRAMS



32-pin, 600-mil DIP



32-pin, 525-mil SOP

ORDERING INFORMATION

