

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

SA701

DESCRIPTION

The SA701 is an advanced dual modulus (Divide By 128/129 or 64/65) low power ECL prescaler. The minimum supply voltage is 2.7V and is compatible with the CMOS UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBIC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package, and is pin compatible with Fujitsu MB501, Plessey SP8704 and Motorola MC12022.

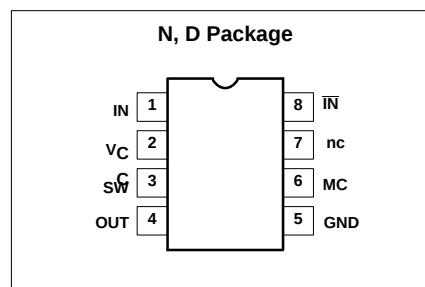
FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA701N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA701D	0174C

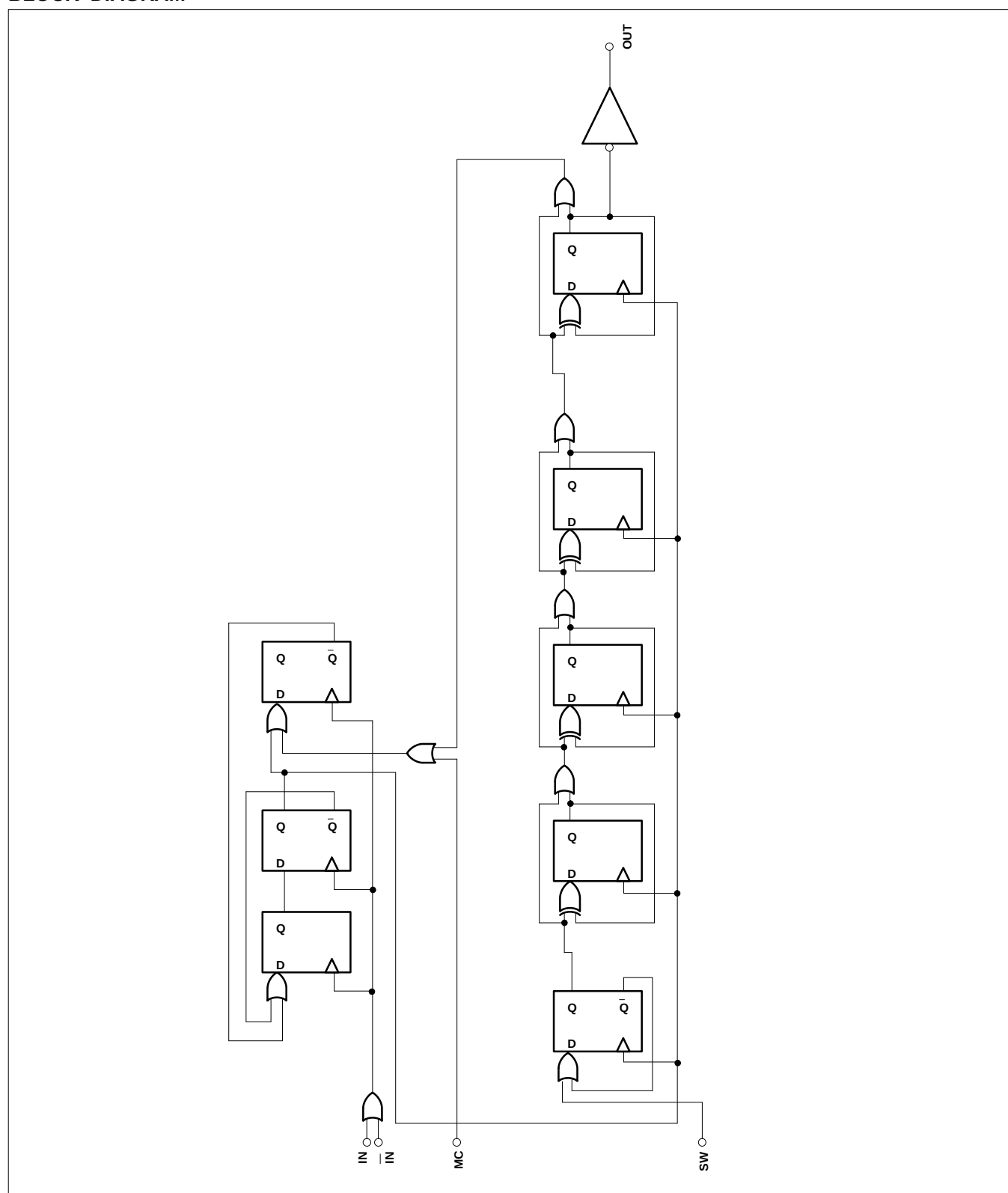
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V _{CC}	Supply voltage	-0.3 to +7.0	V
V _{IN}	Voltage applied to any other pin	-0.3 to (V _{CC} + 0.3)	V
I _O	Output current	10	mA
T _{STG}	Storage temperature range	-65 to +125	°C
T _A	Operating ambient temperature range	-55 to +125	°C
θ _{JA}	Thermal impedance	D package N package	158 108
			°C/W

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BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25^\circ\text{C}$ and $V_{CC} = 3.0\text{V}$; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	$f_{IN} = 1\text{GHz}$, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	$I_{OUT} = 1.2\text{mA}$	$V_{CC}-1.4$			V
V_{OL}	Output low level			$V_{CC}-2.6$		V
V_{IH}	MC input high threshold		2.0		V_{CC}	V
V_{IL}	MC input low threshold		-0.3		0.8	V
V_{IH}	SW input high threshold		2.0		V_{CC}	V
V_{IL}	SW input low threshold		-0.3		0.8	V
I_{IH}	MC input high current	$V_{MC} = V_{CC} = 6\text{V}$		0.1	50	μA
I_{IL}	MC input low current	$V_{MC} = 0\text{V}$, $V_{CC} = 6\text{V}$	-100	-30		μA
I_{IH}	SW input high current	$V_{SW} = V_{CC} = 6\text{V}$		35	100	μA
I_{IL}	SW input low current	$V_{SW} = 0\text{V}$, $V_{CC} = 6\text{V}$	-50	-0.1		μA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for $V_{CC} = 3.0\text{V}$, $f_{IN} = 1\text{GHz}$, input level = 0dBm, $T_A = 25^\circ\text{C}$; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude ¹	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input ²	0		1.1	GHz
		1000pF input coupling			1.1	GHz
R_{ID}	Differential input resistance	DC measurement		5		k Ω
V_O	Output voltage	$V_{CC} = 5.0\text{V}$		1.6		V_{P-P}
		$V_{CC} = 3.0\text{V}$		1.2		V_{P-P}
t_S	Modulus set-up time ¹				5	ns
t_H	Modulus hold time ¹				0	ns
t_{PD}	Propagation time			10		ns

NOTES:

- Maximum limit is not tested, however, it is guaranteed by design and characterization.
- For $f_{IN} < 50\text{MHz}$, minimum input slew rate of $32\text{V}/\mu\text{s}$ is required.

DESCRIPTION OF OPERATION

The SA701 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for SW (Modulus Set Switch) input to be set low and MC (Modulus Control) input to be set high in which case the circuit comprises a divide by 128. For divide by 129 the MC signal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. Similarly, for divide by 64 and 65 the SA701 will generate those respective moduli with the SW signal forced high, in which the fourth stage of the synchronous divider is

bypassed. A truth table for the modulus values is given below:

Table 1.

Modulus	MC	SW
128	1	0
129	0	0
64	1	1
65	0	1

For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to

the input. The rising edge of the output occurs at the count 64 for modulus 128/129 or count 32 for modulus 64/65 with delay t_{PD} . The SW input is not designed for synchronous switching.

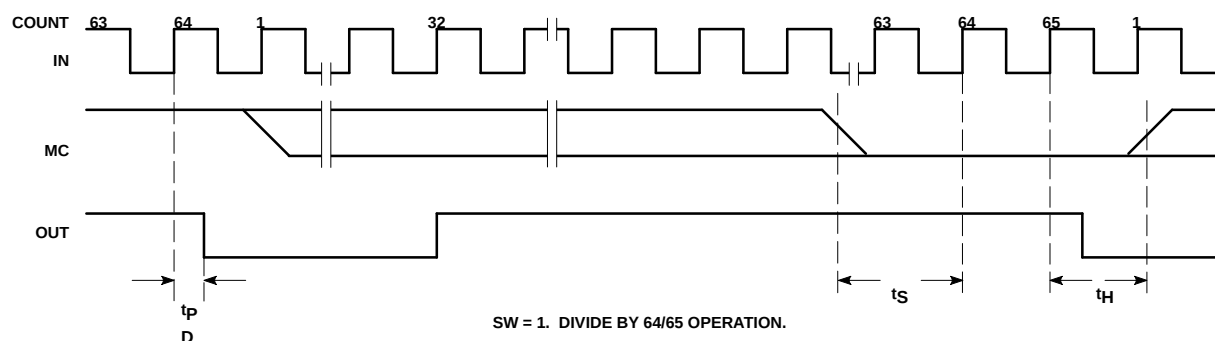
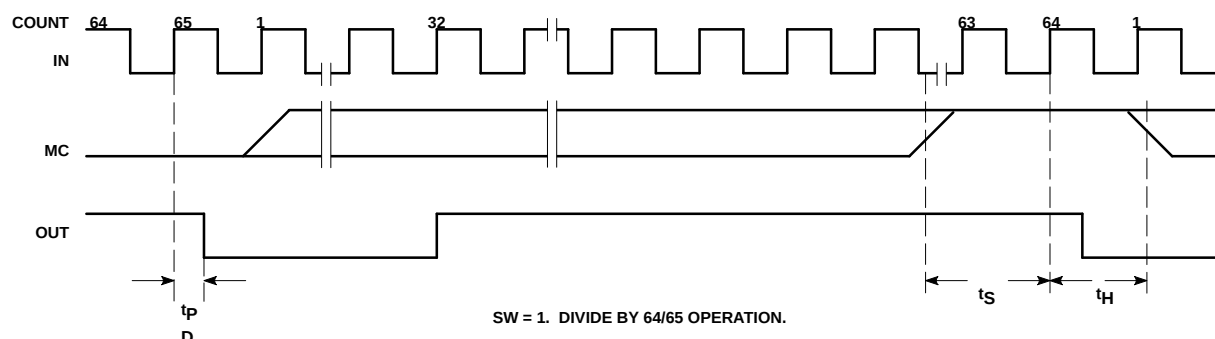
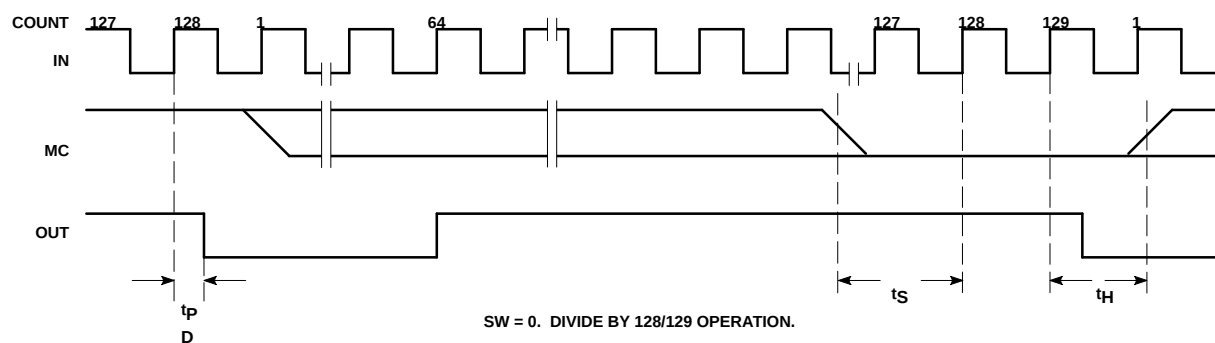
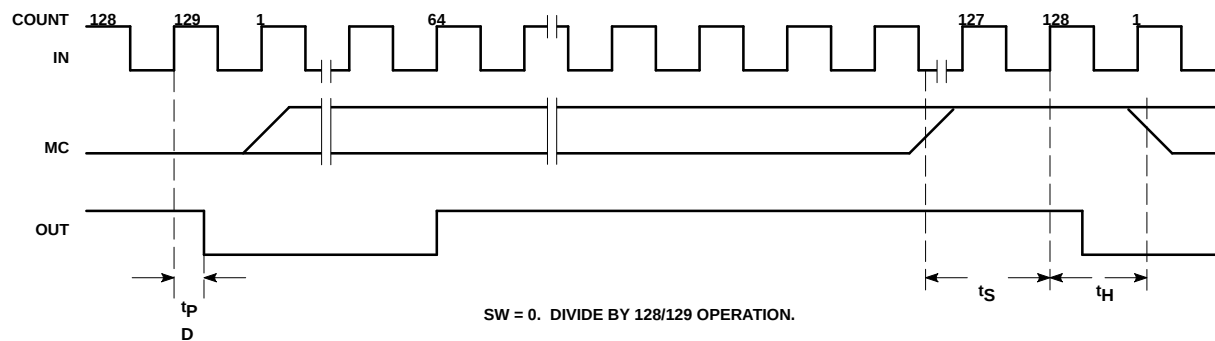
The MC and SW inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed. The SW input has an internal pull-down simplifying modulus group selection. With SW open the divide by 128/129 mode is selected and with SW connected to V_{CC} divide by 64/65 is selected.

The prescaler input is differential and ECL compatible. The output is single-ended ECL compatible.

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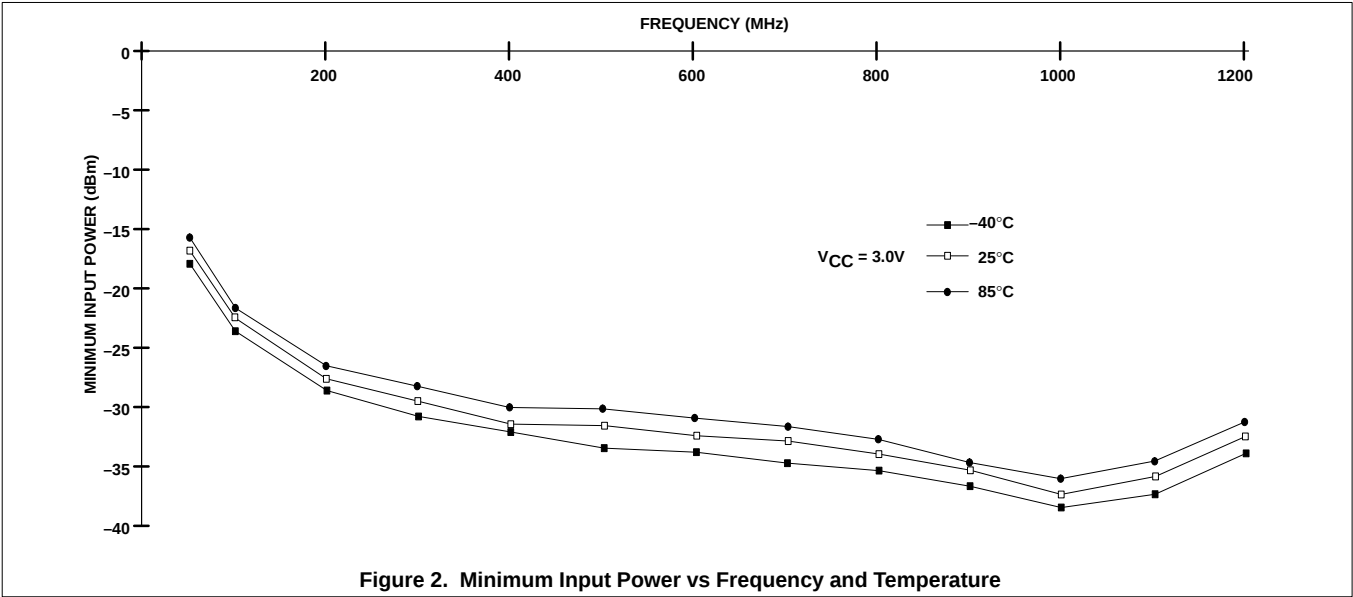
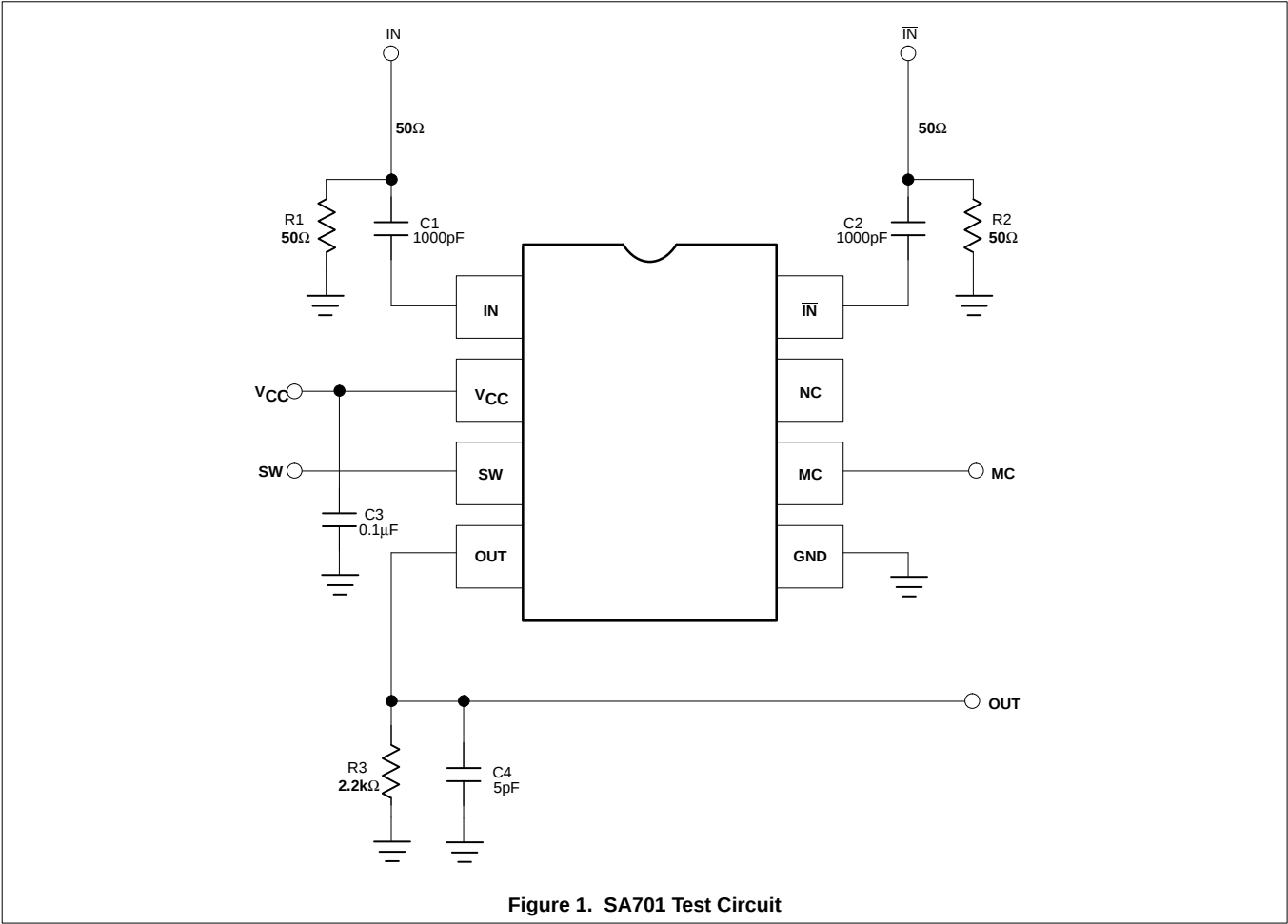
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AC TIMING CHARACTERISTICS



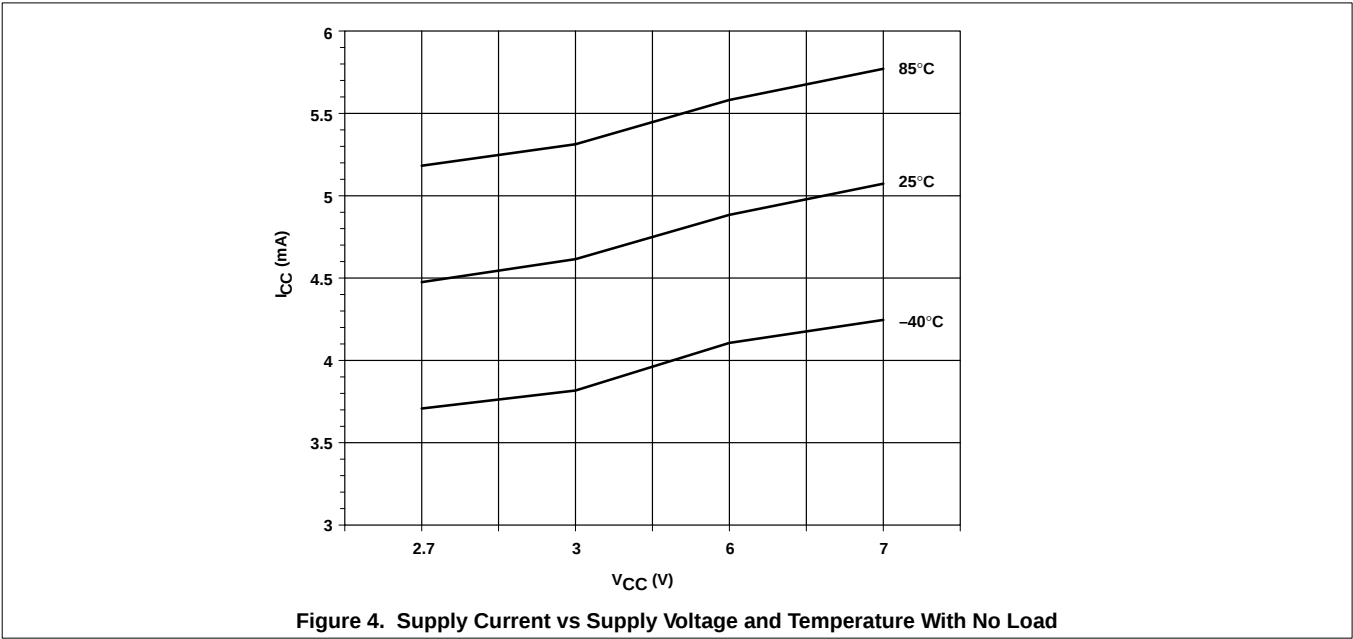
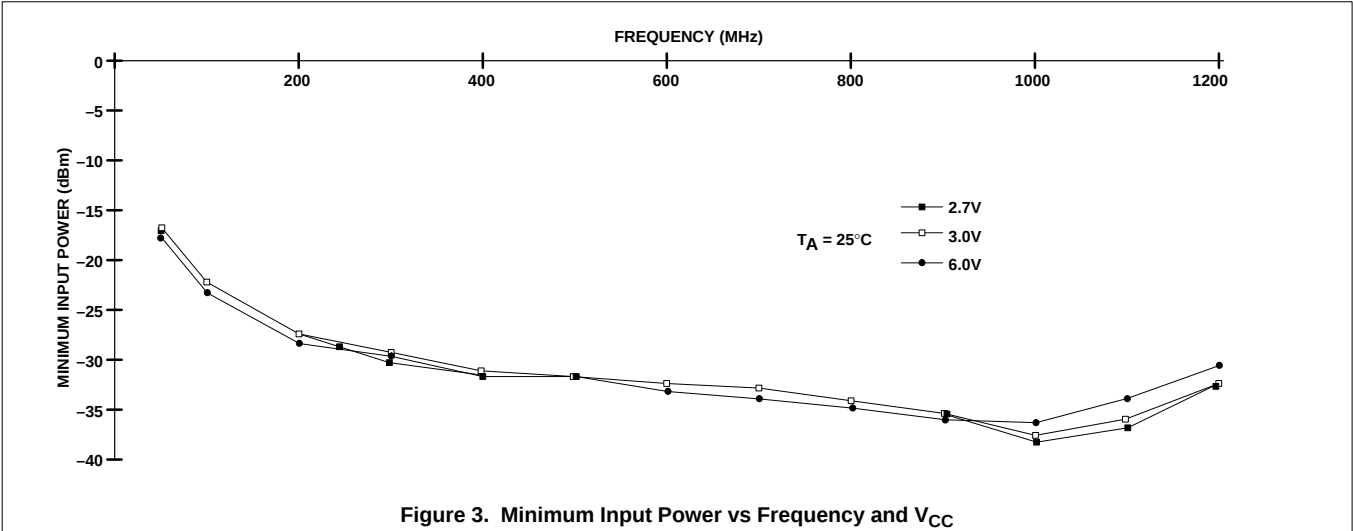
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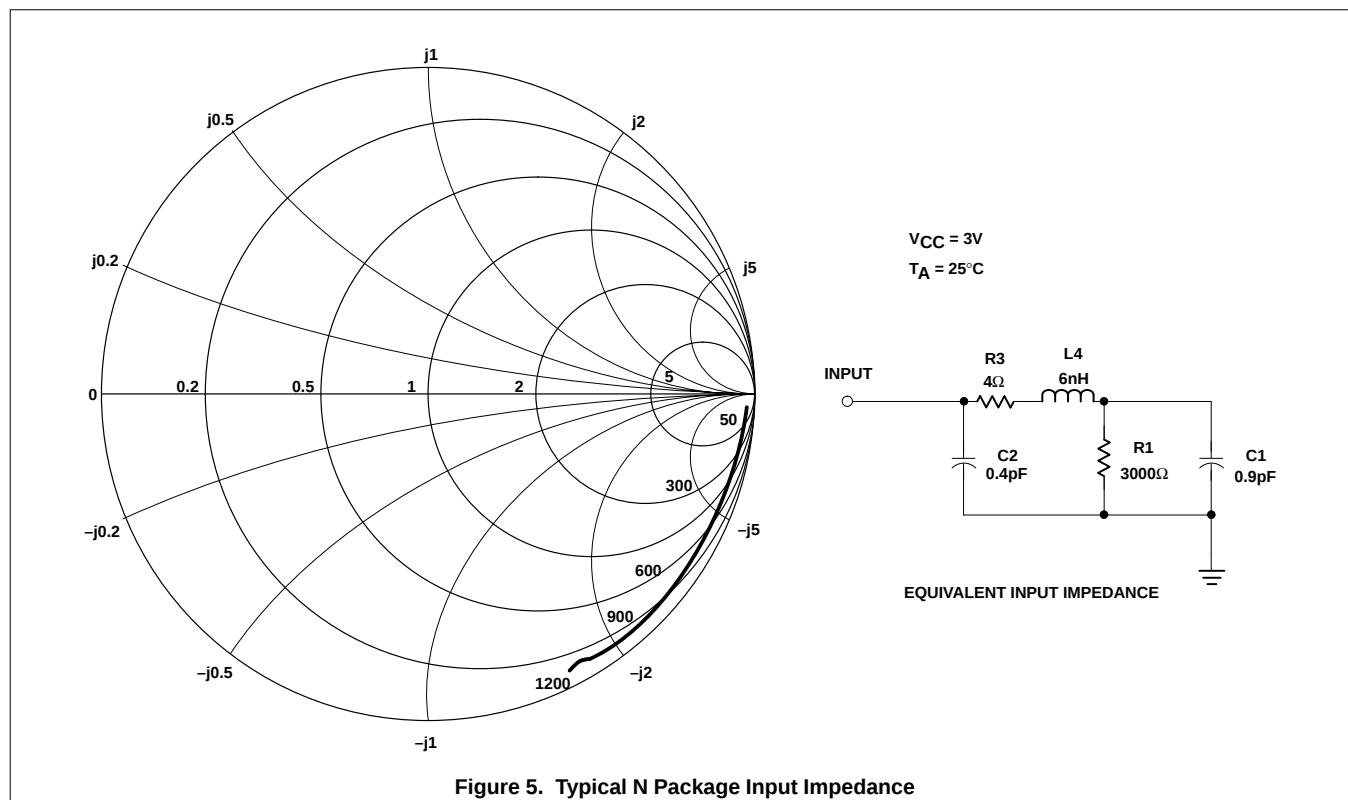


Figure 5. Typical N Package Input Impedance

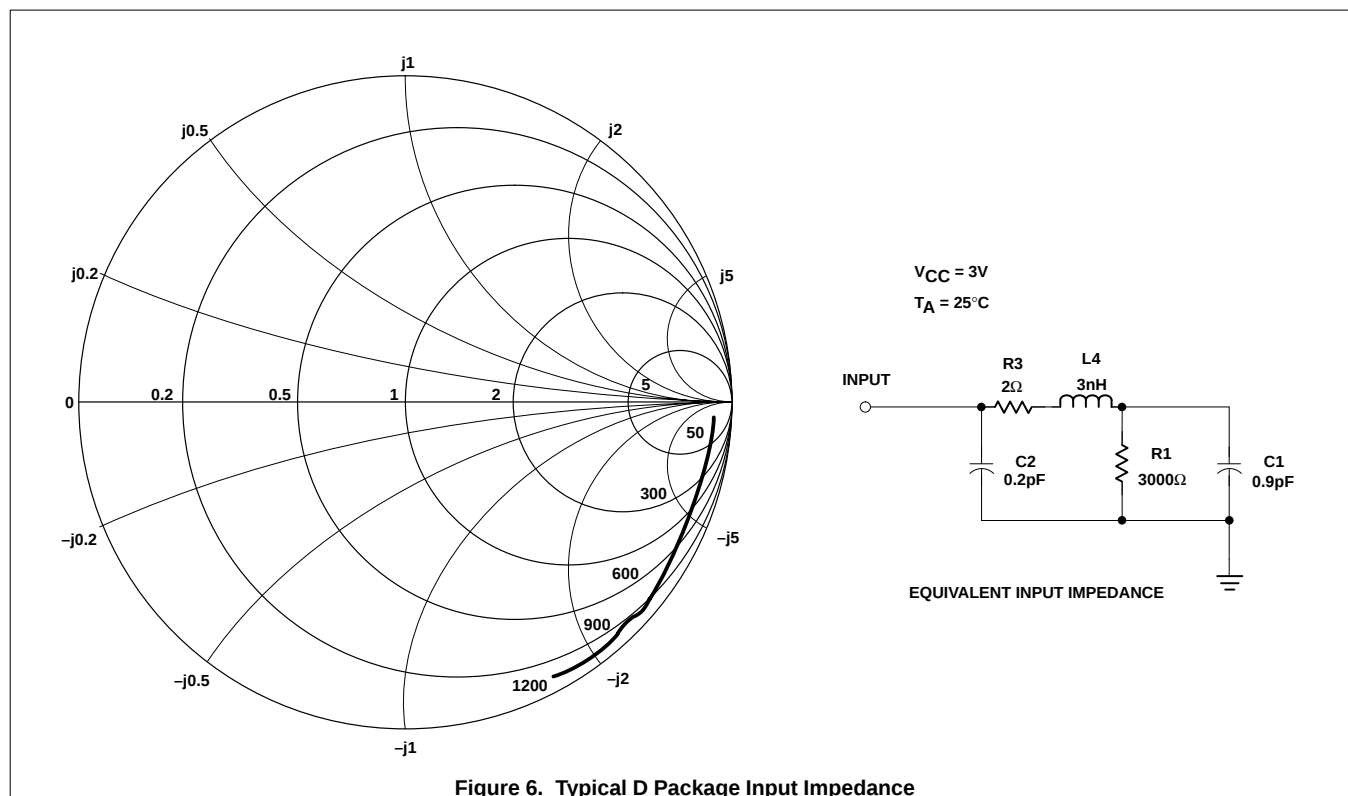


Figure 6. Typical D Package Input Impedance