











**MAX3232E** SLLS664C - AUGUST 2005-REVISED JUNE 2015

# MAX3232E 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver With ±15-kV IEC ESD Protection

#### **Features**

- ESD Protection for RS-232 Bus Pins
  - ±15 kV (HBM)
  - ±8 kV (IEC61000-4-2, Contact Discharge)
  - ±15 kV (IEC61000-4-2, Air-Gap Discharge)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU V.28 Standards
- Operates With 3-V to 5.5-V V<sub>CC</sub> Supply
- Operates up to 250 kbit/s
- Two Drivers and Two Receivers
- Low Supply Current: 300 µA (Typical)
- External Capacitors: 4 x 0.1 µF
- Accepts 5-V Logic Input With 3.3-V Supply
- Pin Compatible to Alternative High-Speed Devices (1 Mbit/s)
  - SN65C3232E (-40°C to +85°C)
  - SN75C3232E (0°C to 70°C)

## Applications

- **Battery-Powered Systems**
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

### 3 Description

The MAX3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND).

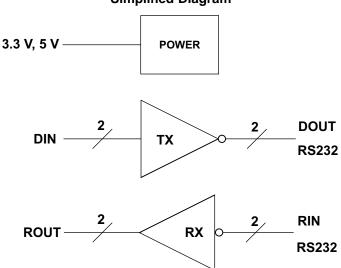
The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MAX3232ExD	SOIC (16)	9.90 mm × 3.91 mm
MAX3232ExDB	SSOP (16)	6.20 mm × 5.30 mm
MAX3232ExDW	SOIC (16)	10.30 mm × 7.50 mm
MAX3232ExPW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Simplified Diagram





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### 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### Changes from Revision B (December 2013) to Revision C

**Page** 

Changes from Revision A (April 2007) to Revision B

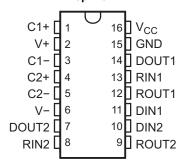
Page

Updated document to new TI data sheet format.
 Deleted Ordering Information table.
 Added Thermal Information table.



# 5 Pin Configuration and Functions

#### D, DW, DB and PW Package 16-Pin SOIC, SSOP and TSSOP Top View



#### **Pin Functions**

	PIN I/O		DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
C1+	1	_	Positive lead of C1 capacitor
V+	2	0	Positive charge pump output for storage capacitor only
C1-	3	_	Negative lead of C1 capacitor
C2+	4	_	Positive lead of C2 capacitor
C2-	5	_	Negative lead of C2 capacitor
V-	6	0	Negative charge pump output for storage capacitor only
DOUT2	7	0	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	0	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
ROUT1	12	0	Logic data output (to UART)
RIN1	13	I	RS232 line data input (from remote RS232 system)
DOUT1	14	0	RS232 line data output (to remote RS232 system)
GND	15	_	Ground
V <sub>CC</sub>	16	_	Supply Voltage, Connect to external 3-V to 5.5-V power supply



# 6 Specifications

#### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		-0.3	6	V
V+	Positive output supply voltage <sup>(2)</sup>		-0.3	7	V
V-	Negative output supply voltage (2)		0.3	<b>-</b> 7	٧
V+ - V-	Supply voltage difference <sup>(2)</sup>			13	V
	land deltana	Drivers	-0.3	6	V
VI	Input voltage	Receivers	-25	25	V
V	Output voltage	Drivers	-13.2	13.2	V
Vo	Output voltage	Receivers	-0.3	$V_{CC} + 0.3$	٧
TJ	Operating virtual junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 6.2 ESD Ratings

				VALUE	UNIT
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except RIN and DOUT	±2000		
		ANSI/ESDA/JEDEC JS-001(*)	RIN and DOUT Pins	±15,000	
V <sub>(ESD)</sub> Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	All pins	±1500	V	
	(ESD)	IEC61000-4-2, Contact Discharge	RS232 port pins (RIN, DOUT)	±8000	
		IEC61000-4-2, Air-Gap Discharge	RS232 port pins (RIN, DOUT)	±15,000	

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

# 6.3 Recommended Operating Conditions<sup>(1)</sup>

See Figure 7.

				MIN	NOM	MAX	UNIT
	Supply voltage		$V_{CC} = 3.3 \text{ V}$	3	3.3	3.6	V
	Supply voltage		$V_{CC} = 5 V$	4.5	5	5.5	
	$V_{IH}$ Driver high-level input voltage DIN $ \frac{V_{CC} = 3.3 \text{ V}}{V_{CC} = 5 \text{ V}} $	DIN	$V_{CC} = 3.3 \text{ V}$	2		5.5	V
VIH		DIN	$V_{CC} = 5 V$	2.4		5.5	V
$V_{IL}$	Driver low-level input voltage	DIN		0		8.0	V
$V_{I}$	Receiver input voltage	RIN		-25		25	V
_		MAX3232EC	0		70	°C	
T <sub>A</sub>	Operating free-air temperature		MAX3232EI	-40		85	30

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at  $V_{CC}$  = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at  $V_{CC}$  = 5 V ± 0.5 V.

<sup>(2)</sup> All voltages are with respect to network GND.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



#### 6.4 Thermal Information

			MAX3232E				
	THERMAL METRIC <sup>(1)</sup>	PW (TSSOP)	D (SOIC)	DW (SOIC)	DB (SSOP)	UNIT	
		16 PINS	16 PINS	16 PINS	16 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.3	76.1	72.3	90.9	°C/W	
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	20.8	36.7	33.5	36.2	°C/W	
$R_{\theta JB}$	Junction-to-board thermal resistance	45.1	33.6	37.1	43.8	°C/W	
ΨЈТ	Junction-to-top characterization parameter	0.6	4.2	7.5	4.2	°C/W	
ΨЈВ	Junction-to-board characterization parameter	45.1	33.3	37.1	42.9	°C/W	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	_	_	_	_	°C/W	

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

### 6.5 Electrical Characteristics — Device<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 7).

PARAMETER	TEST CONDITIONS	MIN TYP <sup>(2)</sup> MAX	UNIT
CC Supply current	No load, $V_{CC} = 3.3 \text{ V or 5 V}$	0.3 1	mA

Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V. All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.6 Electrical Characteristics — Driver<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted) (see Figure 7).

	PARAMETER	TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND,	DIN = GND	5	5.4		V
$V_{OL}$	Low-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND,	$DIN = V_{CC}$	-5	-5.4		V
I <sub>IH</sub>	High-level input current	$V_I = V_{CC}$			±0.01	±1	μΑ
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> at GND			±0.01	±1	μΑ
I <sub>OS</sub> (3)	Short-circuit output current	V <sub>CC</sub> = 3.6 V,	$V_O = 0 V$	0.5		00	mA
los (°/	Short-circuit output current	V <sub>CC</sub> = 5.5 V,	$V_O = 0 V$		±35	±60	MA
r <sub>O</sub>	Output resistance	$V_{CC}$ , V+, and V- = 0 V,	$V_O = \pm 2 V$	300	10M		Ω

Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

## 6.7 Electrical Characteristics — Receiver<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 7).

	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -1 \text{ mA}$	V <sub>CC</sub> - 0.6	$V_{CC} - 0.1$		V
$V_{OL}$	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
V Desitive resident in most through and waltered	V <sub>CC</sub> = 3.3 V		1.5	2.4	V	
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 5 V		1.8	2.4	V
.,	Negative going input threehold valtage	V <sub>CC</sub> = 3.3 V	0.6	1.2		\/
V <sub>IT</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 5 V	0.8	1.5		V
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.3		V
rį	Input resistance	$V_I = \pm 3 \text{ V to } \pm 25 \text{ V}$	3	5	7	kΩ

Test conditions are C1–C4 = 0.1  $\mu$ F at  $V_{CC}$  = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at  $V_{CC}$  = 5 V  $\pm$  0.5 V.

Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25 ^{\circ}\text{C}$ .

All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25 ^{\circ}\text{C}$ .



# 6.8 Switching Characteristics(1)

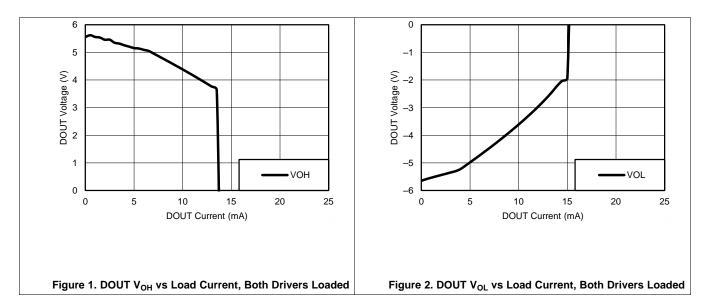
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 7)

	PARAMETER	TEST CONDITIONS			TYP <sup>(2)</sup>	MAX	UNIT
	Maximum data rate	$R_L = 3 \text{ k}\Omega$ , One DOUT switching,	C <sub>L</sub> = 1000 pF, see Figure 3	150	250		kbit/s
t <sub>sk(p)</sub>	Driver pulse skew <sup>(3)</sup>	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega,$ see Figure 4	$C_L = 150 \text{ pF to } 2500 \text{ pF},$		300		ns
	Driver slew rate, transition	$R_1 = 3 k\Omega$ to $7 k\Omega$ ,	C <sub>L</sub> = 150 pF to 1000 pF	6		30	
SR(tr)	r) region (see Figure 3) $V_{CC} = 3.3 \text{ V}$		C <sub>L</sub> = 150 pF to 2500 pF	4		30	V/µs
t <sub>PLH</sub>	Receiver propagation delay time, low- to high-level output	$C_L = 150 \text{ pF},$			300		ns
t <sub>PHL</sub>	Receiver propagation delay time, high- to low-level output	see Figure 5			300		ns
t <sub>sk(p)</sub>	Receiver pulse skew <sup>(3)</sup>				300		ns

- Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V ± 0.5 V. All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C. Pulse skew is defined as  $|t_{PLH} t_{PHL}|$  of each channel of the same device.

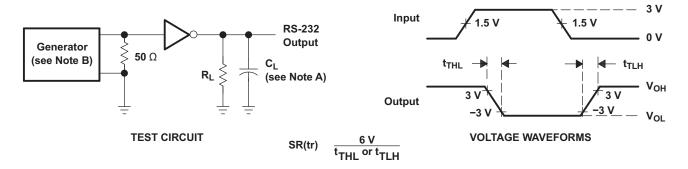
# 6.9 Typical Characteristics

 $V_{CC} = 3.3 \text{ V}$ 



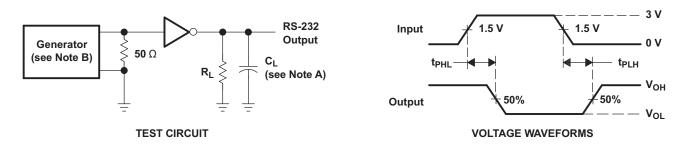


#### 7 Parameter Measurement Information



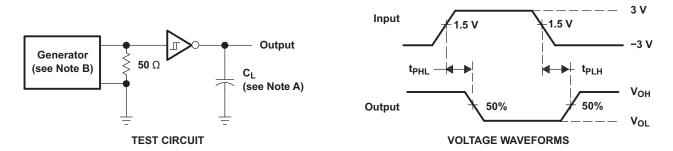
- A. C<sub>L</sub> includes probe and jig capacitance
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O$  = 50  $\Omega$ , 50% duty cycle,  $t_r \le 10$  ns,  $t_f \le 10$  ns

Figure 3. Driver Slew Rate



- A. C<sub>L</sub> includes probe and jig capacitance
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O$  = 50  $\Omega$ , 50% duty cycle,  $t_r \le 10$  ns,  $t_f \le 10$  ns

Figure 4. Driver Pulse Skew



- A. C<sub>L</sub> includes probe and jig capacitance
- B. The pulse generator has the following characteristics:  $Z_0 = 50 \Omega$ , 50% duty cycle,  $t_r \le 10$  ns,  $t_f \le 10$  ns

Figure 5. Receiver Propagation Delay Times

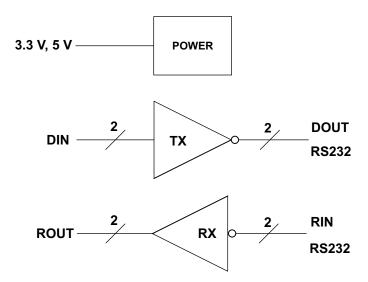


### 8 Detailed Description

#### 8.1 Overview

The MAX3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with IEC61000-4-2 ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate. Outputs are protected against shorts to ground.

#### 8.2 Functional Block Diagram



#### 8.3 Feature Description

#### 8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V- pins using a charge pump that requires four external capacitors.

#### 8.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

#### 8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.



#### 8.4 Device Functional Modes

Table 1 and Table 2 list the functional modes of the drivers and receivers of MAX3232E.

Table 1. Each Driver<sup>(1)</sup>

INPUT DIN	OUTPUT DOUT
L	Н
Н	L

(1) H = high level, L = low level

Table 2. Each Receiver<sup>(1)</sup>

INPUT RIN	OUTPUT ROUT
L	Н
Н	L
Open	Н

H = high level, L = low level,
 Open = input disconnected or connected driver off

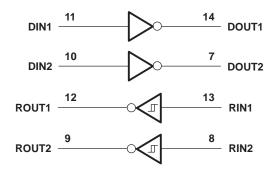


Figure 6. Logic Diagram

#### 8.4.1 V<sub>CC</sub> Powered by 3 V to 5.5 V

The device is in normal operation.

#### 8.4.2 $V_{CC}$ Unpowered, $V_{CC} = 0 \text{ V}$

When MAX3232E is unpowered, it can be safely connected to an active remote RS232 device.

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## 9 Applications and Implementation

#### NOTE

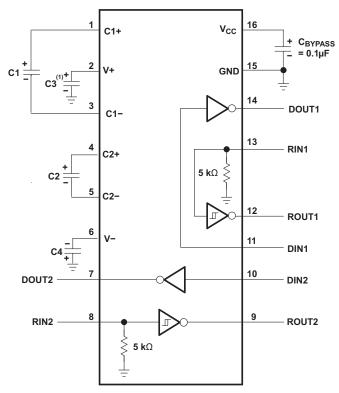
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 9.1 Application Information

For proper operation, add capacitors as shown in Table 3.

#### 9.2 Typical Application

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.



(1) C3 can be connected to V<sub>CC</sub> or GND

Notes: A. Resistor values shown are nominal.

B. Nonpolorized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 7. Typical Operating Circuit and Capacitor Values

 V<sub>CC</sub>
 C1
 C2, C3, C4

 3.3 V ± 0.3 V
 0.1 μF
 0.1 μF

 5 V ± 0.5 V
 0.047 μF
 0.33 μF

**Table 3. VCC vs Capacitor Values** 

 $0.1 \mu F$ 

Submit Documentation Feedback

 $3 V \pm 5.5 V$ 

 $0.47 \mu F$ 



#### 9.2.1 Design Requirements

The recommended  $V_{CC}$  is 3.3 V or 5 V. 3 V to 5.5 V is also possible

The maximum recommended bit rate is 250 kbit/s.

#### 9.2.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on  $V_{\text{CC}}$  level for best performance.

#### 9.2.3 Application Curve

Figure 8 curves are for 3.3-V VCC and 250-kbit/s alternative bit data stream.

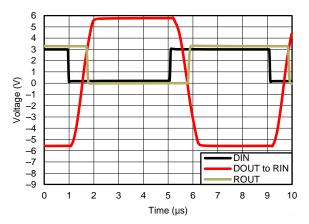


Figure 8. 250 kbit/s Driver to Receiver Loopback Timing Waveform,  $V_{\text{CC}}$ = 3.3 V



### 10 Power Supply Recommendations

The supply voltage,  $V_{CC}$ , should be between 3 V and 5.5 V. Select the values of the charge-pump capacitors using Table 3.

#### 11 Layout

#### 11.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

#### 11.2 Layout Example

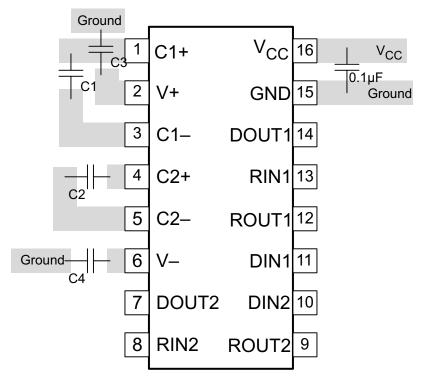


Figure 9. Layout Diagram



# 12 Device and Documentation Support

#### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.2 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

#### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 12.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.





8-Nov-2014

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3232ECD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	Samples
MAX3232ECDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples
MAX3232ECDBE4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples
MAX3232ECDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples
MAX3232ECDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples
MAX3232ECDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples
MAX3232ECDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	Samples
MAX3232ECDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	Samples
MAX3232ECDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	Samples
MAX3232ECDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	Samples
MAX3232ECDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	Samples
MAX3232ECDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	Samples
MAX3232ECDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	Samples
MAX3232ECDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	Samples
MAX3232ECPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples
MAX3232ECPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples
MAX3232ECPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples





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Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3232ECPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples
MAX3232ECPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples
MAX3232ECPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	Samples
MAX3232EID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	Samples
MAX3232EIDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples
MAX3232EIDBE4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples
MAX3232EIDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples
MAX3232EIDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples
MAX3232EIDBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples
MAX3232EIDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples
MAX3232EIDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	Samples
MAX3232EIDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	Samples
MAX3232EIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	Samples
MAX3232EIDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	Samples
MAX3232EIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	Samples
MAX3232EIDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	Samples
MAX3232EIDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	Samples
MAX3232EIDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	Samples



## PACKAGE OPTION ADDENDUM

8-Nov-2014

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3232EIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples
MAX3232EIPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples
MAX3232EIPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples
MAX3232EIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples
MAX3232EIPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



# PACKAGE OPTION ADDENDUM

8-Nov-2014

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#### OTHER QUALIFIED VERSIONS OF MAX3232E:

Automotive: MAX3232E-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# PACKAGE MATERIALS INFORMATION

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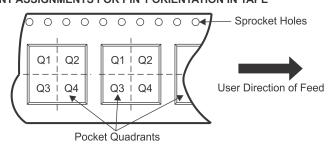
## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3232ECDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
MAX3232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX3232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3232EIDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
MAX3232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX3232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3232ECDBR	SSOP	DB	16	2000	367.0	367.0	38.0
MAX3232ECDR	SOIC	D	16	2500	367.0	367.0	38.0
MAX3232ECDWR	SOIC	DW	16	2000	367.0	367.0	38.0
MAX3232ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX3232EIDBR	SSOP	DB	16	2000	367.0	367.0	38.0
MAX3232EIDR	SOIC	D	16	2500	367.0	367.0	38.0
MAX3232EIDWR	SOIC	DW	16	2000	367.0	367.0	38.0
MAX3232EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

# D (R-PDS0-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

DW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



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MAX3232ECPW MAX3232ECPWE4 MAX3232ECPWR MAX3232ECPWRE4 MAX3232EID MAX3232EIDB
MAX3232EIDBE4 MAX3232EIDBR MAX3232EIDBRE4 MAX3232EIDE4 MAX3232EIDR MAX3232EIDRE4
MAX3232EIDW MAX3232EIDWR MAX3232EIPW MAX3232EIPWE4 MAX3232EIPWR MAX3232EIPWRE4
MAX3232ECDBG4 MAX3232ECDBRG4 MAX3232ECDG4 MAX3232ECDRG4 MAX3232ECDWG4
MAX3232ECDWRG4 MAX3232ECPWG4 MAX3232ECPWRG4 MAX3232EIDBRG4
MAX3232EIDG4 MAX3232EIDRG4 MAX3232EIDWG4 MAX3232EIDWRG4