DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40174B
MSI
Hex D-type flip-flop

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Hex D-type flip-flop

HEF40174B
MSI

DESCRIPTION

The HEF40174B is a hex edge-triggered D-type flip-flop with six data inputs (D_0 to D_5), a clock input (CP), an overriding asynchronous master reset input ($\overline{MR}$), and six buffered outputs (O_0 to O_5). Information on D_0 to D_5 is transferred to O_0 to O_5 on the LOW to HIGH transition of CP if $\overline{MR}$ is HIGH. When LOW, $\overline{MR}$ resets all flip-flops (O_0 to O_5 = LOW) independent of CP and D_0 to D_5.

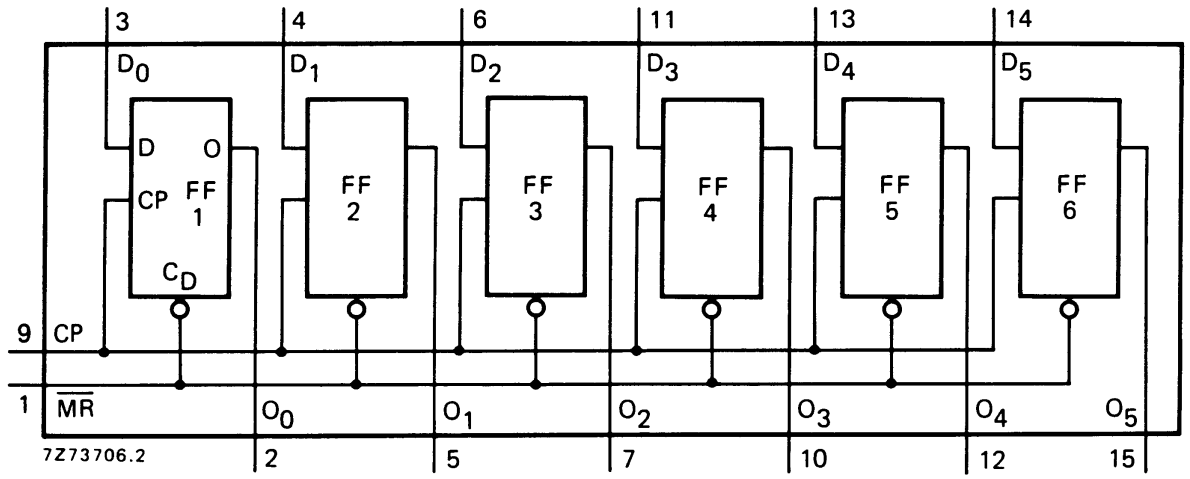


Fig.1 Functional diagram.

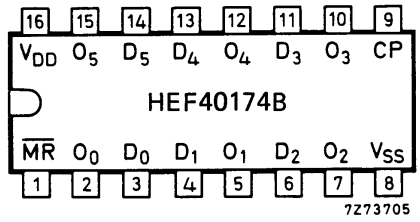


Fig.2 Pinning diagram.

HEF40174BP(N): 16-lead DIL; plastic (SOT38-1)
HEF40174BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF40174BT(D): 16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

PINNING

D_0 to D_5	data inputs
CP	clock input (LOW to HIGH; edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_5	buffered outputs

FUNCTION TABLE

INPUTS			OUTPUT
CP	D	$\overline{MR}$	O
⌐¯	H	H	H
⌐¯	L	H	L
¯⌐	X	H	no change
X	X	L	L

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   ⌐¯ = positive-going transition
   ¯⌐ = negative-going transition

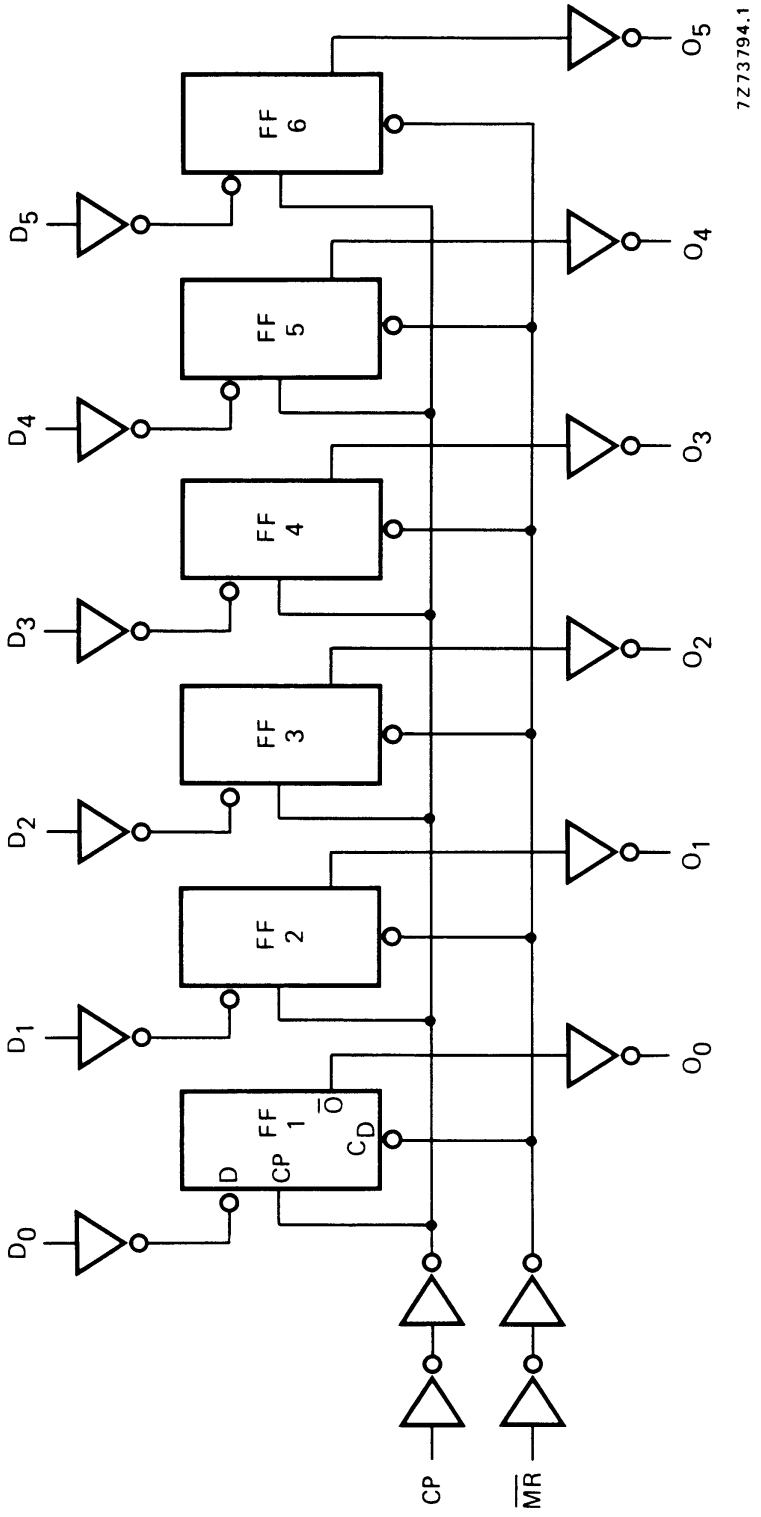


Fig.3 Logic diagram.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
CP → O_n	5			75	155	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	65	ns	19 ns + (0,23 ns/pF) C_L
	15			20	45	ns	12 ns + (0,16 ns/pF) C_L
	5			75	155	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	65	ns	19 ns + (0,23 ns/pF) C_L
	15			20	45	ns	12 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → O_n	5			85	175	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time	5		20	10		ns	see also waveforms Fig.4
D_n → CP	10	t_{su}	10	5		ns	
	15		10	5		ns	
Hold time	5		10	0		ns	
D_n → CP	10	t_{hold}	5	0		ns	
	15		5	0		ns	
Minimum clock	5		70	35		ns	
pulse width; LOW	10	t_{WCPL}	30	15		ns	
	15		20	10		ns	
Minimum $\overline{MR}$ pulse	5		70	35		ns	
width; LOW	10	t_{WMRL}	35	15		ns	
	15		25	10		ns	
Recovery time	5		45	25		ns	
for $\overline{MR}$	10	t_{RMR}	20	10		ns	
	15		15	5		ns	
Maximum clock	5		5	11		MHz	
pulse frequency	10	f_{max}	15	30		MHz	
	15		20	45		MHz	

	V_{DD} V	TYPICAL FORMULA FOR P(μW)	
Dynamic power dissipation per package (P)	5	$3500\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$16\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$42\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	

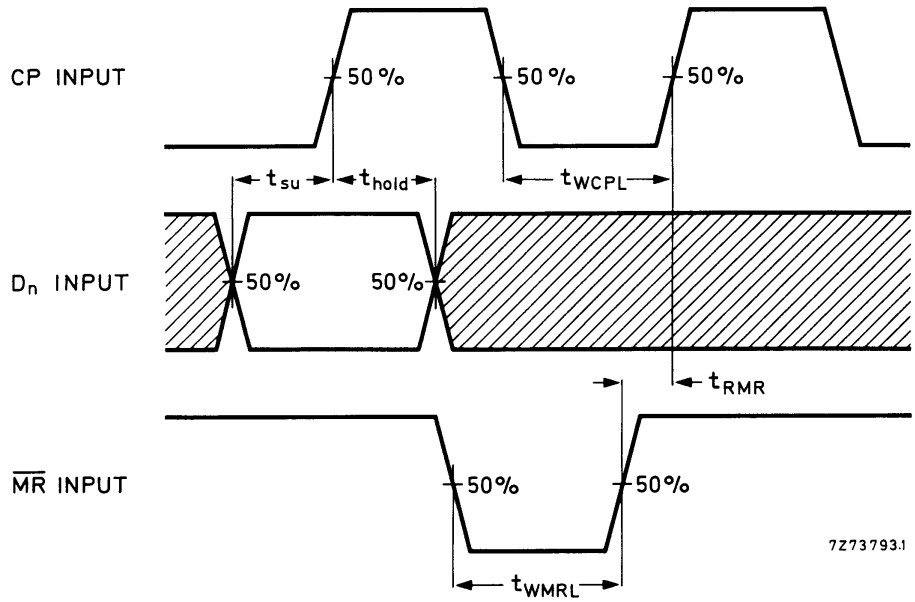


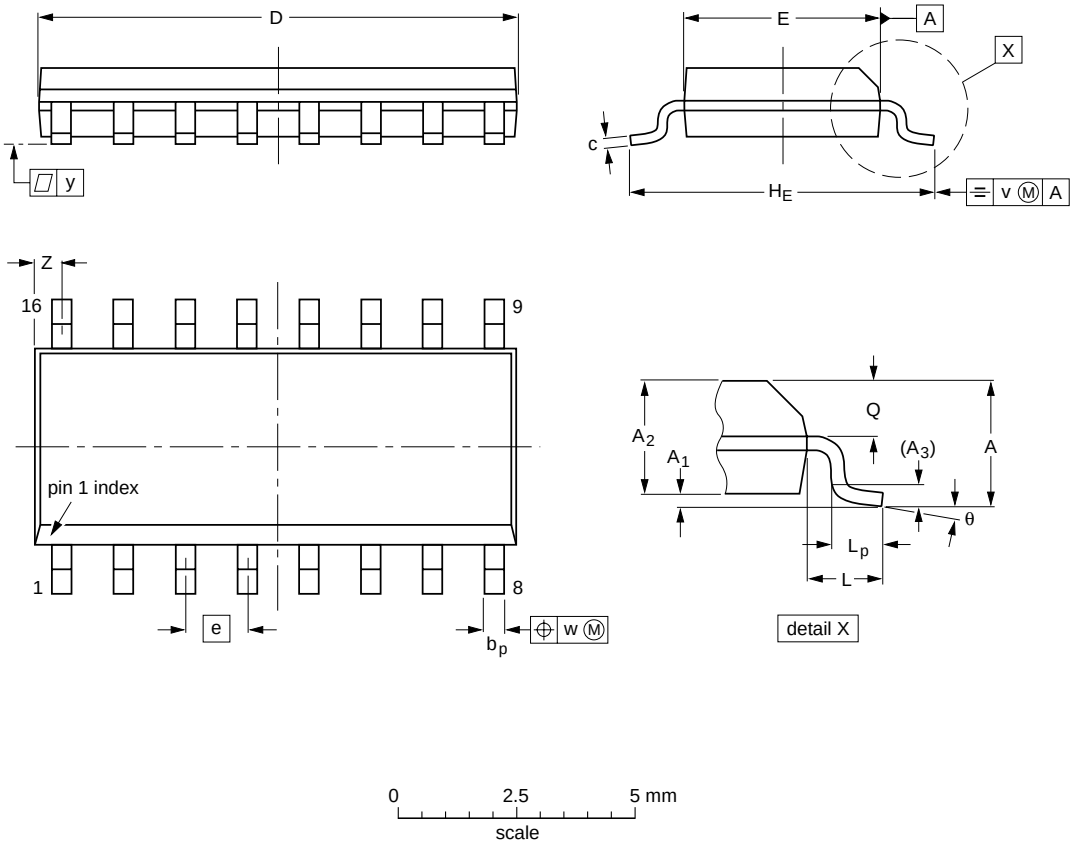
Fig.4 Waveforms showing minimum pulse widths for CP and $\overline{MR}$, $\overline{MR}$ to CP recovery time, and set-up time and hold time for D_n to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40174B are:

- Shift registers
- Buffer/storage register
- Pattern generator

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

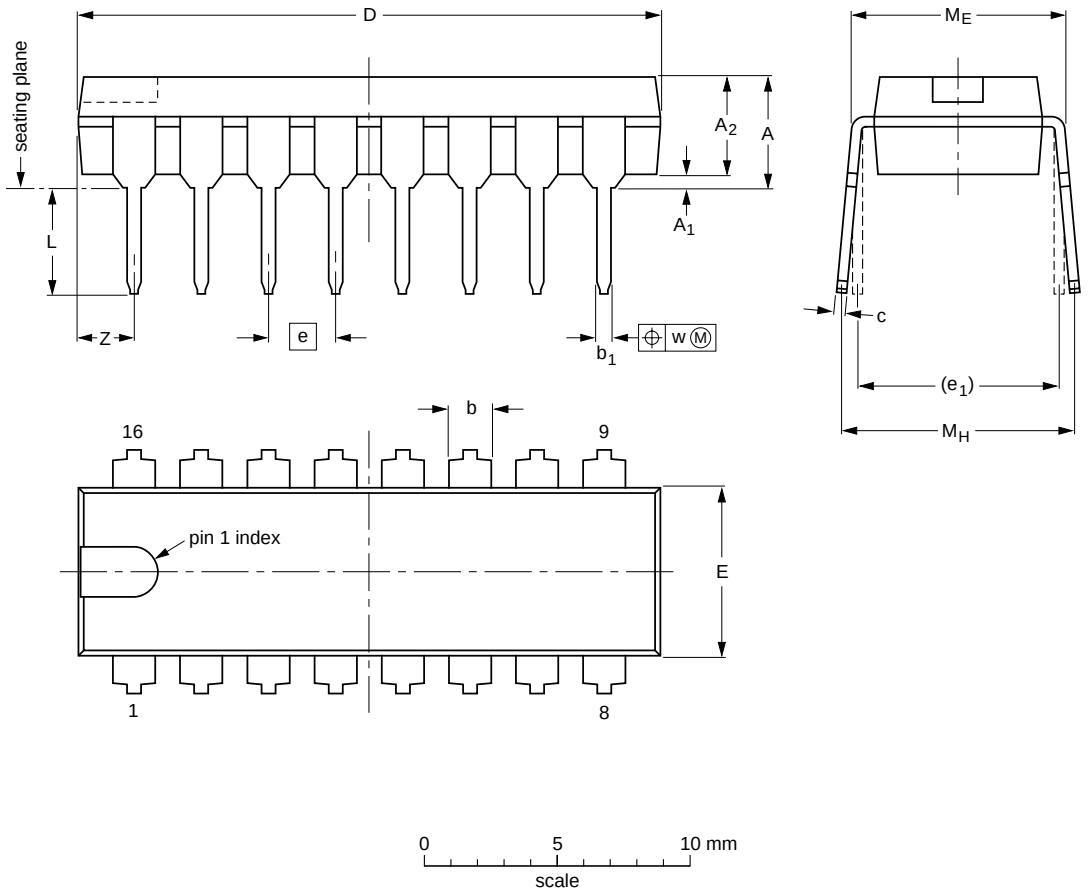
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19